Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances

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Transparent electronics is today one of the most advanced topics for a wide range of device applications. The key components are wide bandgap semiconductors, where oxides of different origins play an important role, not only as passive component but also as active component, similar to what is observed in conventional semiconductors like silicon. Transparent electronics has gained special attention during the last few years and is today established as one of the most promising technologies for leading the next generation of flat panel display due to its excellent electronic performance. In this paper the recent progress in n- and p-type oxide based thin-film transistors (TFT) is reviewed, with special emphasis on solution-processed and p-type, and the major milestones already achieved with this emerging and very promising technology are summarizeed. After a short introduction where the main advantages of these semiconductors are presented, as well as the industry expectations, the beautiful history of TFTs is revisited, including the main landmarks in the last 80 years, finishing by referring to some papers that have played an important role in shaping transparent electronics. Then, an overview is presented of state of the art n-type TFTs processed by physical vapour deposition methods, and finally one of the most exciting, promising, and low cost but powerful technologies is discussed: solution-processed oxide TFTs. Moreover, a more detailed focus analysis will be given concerning p-type oxide TFTs, mainly centred on two of the most promising semiconductor candidates: copper oxide and tin oxide. The most recent data related to the production of complementary metal oxide semiconductor (CMOS) devices based on n- and p-type oxide TFT is also be presented. The last topic of this review is devoted to some emerging applications, finalizing with the main conclusions. Related work that originated at CENIMAT|I3N during the last six years is included in more detail, which has led to the fabrication of high performance n- and p-type oxide transistors as well as the fabrication of CMOS devices with and on paper.

1. Introduction

Oxide semiconductors, especially the amorphous ones, are a promising class of TFT materials that have made an impressive progress particularly in display applications in a relatively short time,[1] challenging silicon not only in conventional applications but opening doors to completely new and disruptive areas like paper electronics.[2,3] The key issues here are the ability to produce such semiconductors at low process temperatures and to have highly smooth surfaces, characteristic of amorphous structures, whose electronic performances do not depend on the degree of films disorder.[4] This new class of semiconductor materials, amorphous oxides semiconductors (AOS) represent a revolutionary idea and exhibit a stimulating combination of high optical transparency, high electron mobility and amorphous microstructure.[5,6] Besides that, AOSs do not have grain boundaries, thereby obviating the primary limitation of mobility in polycrystalline semiconductors, which is a huge advantage for process integration. Other advantages include low temperature deposition routes and ultrasmooth surfaces for suppressing interface traps and scattering centres. Besides the advantages of this new technology like the capability for providing real solutions and overcoming many obstacles and limitations of the conventional silicon technology, the used materials as well as the technology itself are environmental friendly and much less expensive.[7]

Although some initial attempts during the 60s were done for SnO_2[8] and ZnO[9] TFT channel layers, only forty years later, with the work of Hosono,[10] Wager,[11] Carcia[12] and Fortunato[13] a significant worldwide interest appeared, especially for active matrix for organic light emitting diodes (AMOLED) technology, both in academia and industry. Besides the demonstration of display prototypes since 2005 by several companies (Toppan Printing, Samsung Electronics, LG Electronics, AU Optronics, among others), Samsung has released at the end of 2010 what they boast proudly as one of the world's finest and largest 3D Ultra Definition (UD) TV with 70" diagonal and a sports resolution of 240 Hz that will meet the demands of 3D capability. Samsung has claimed that the making of this device is the first of the kind on oxide semiconductor TFT technology that supports high pixel density, with a resolution of 3840 × 2160, which is equivalent to 8 MP. Although the first transparent display has

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been done using the conventional a-Si:H technology in 2005 by J. Jang et al.[14] only very recently Samsung announced the mass production of transparent liquid crystal display (LCD) panels, which enables a person to look right through the panel like glass, and it consumes 90% less electricity when compared to a conventional LCD panel using back light unit. This can be achieved because a transparent LCD panel utilizes ambient light such as sunlight, which consequently reduces the dependency on electricity for generating power.

As expected from the already obtained results, the future of transparent electronics seems very promising, since from the last available display market forecast by Displaybank,[15] transparent display would debut the market for the first time in 2012 and sharply grow to create $87.2 billion market by year 2025 as can been seen in the semi-logarithmic plot in **Figure 1**.

Table 1 presents a summary and comparison of some of the most important device properties for the different available technologies: oxide semiconductors; amorphous Si; low temperature polycrystalline Si and organic semiconductors.

2. History of Oxide TFTs

The history of TFTs is the oldest one concerning electronic devices and has more than 80 years. The invention of the TFT occurred in 1925 and was patented in 1930 by J.E. Lilienfeld[21–23] and O. Heil,[24] but at that time little was known about semiconductor materials and vacuum techniques to produce thin films. Therefore, these first reports are actually concept patents and no evidence exists about the production of devices. Still, in these patents, the idea of controlling the current flow in a material by the influence of a transversal electrical field was already present. One of Lilienfeld first patents, published in 1930, describes the basic principle of what is known today as the metal-semiconductor field-effect transistor (MESFET, **Figure 2**a), while other, published three years later, already shows the concept of a device where an insulating material (aluminium oxide) is introduced between the semiconductor (cooper sulfide) and the field-effect electrode (aluminium), anticipating the so-called metal-insulator-semiconductor field-effect transistor (MISFET, Figure 2b).[25] It is also noteworthy that in the MISFET patent,

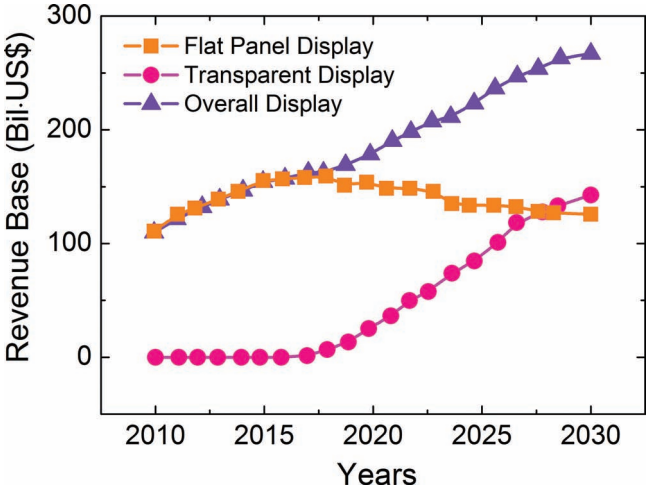


Figure 1. Transparent display technology evolution and global display market (from Displaybank[15]).

Elvira Fortunato received her PhD degree in Physics and Materials Science in 1995 at Universidade Nova de Lisboa. She has been a Full Professor since 2012 in the Materials Science Department of the same University and has been director of the Materials Research Centre (CENIMAT) since 1998. Fortunato pioneered European research on transparent electronics, namely thin-film transistors based on oxide semiconductors, demonstrating that oxide materials may be used as true semiconductors.

Pedro Barquinha received the PhD degree from Universidade Nova de Lisboa in 2010, in Nanotechnologies and Nanosciences, with the dissertation "Transparent Oxide Thin-Film Transistors". His current research topics are the study of materials for transparent/flexible TFTs and integration in circuits, as well as the nanofabrication of devices using FIB/EBL.

Rodrigo Martins received his MSc degree in Amorphous Semiconductor Technologies in 1977, supervised by W. Spear of Dundee University/Scotland. He got the PhD degree in Semiconductors (1982) and in 1988 the *Aggregation* in Microelectronics, by Universidade Nova de Lisboa. He is Full Professor in Microelectronics and Optoelectronics since 2001 in the Materials Science Department of the same University and the head of department since 1996. In 1989 found the Centre of Excellence in Microelectronics and Optoelectronics (CEMOP/Uninova) and in 1993 the research material's center, CENIMAT. Since 2004 he is a member of the executive committees of the European Materials Research Society (EMRS) and of the European Materials Forum (EMF) and, since May 2011 the running president of E-MRS. He is one of the inventors of the paper and memory transistor and of the electrochromic transistor.

Table 1. Comparison between oxide semiconductor TFTs and the other available technologies.[16–20]

TFT properties	Oxide semiconductors	Amorphous Si	Low-T poly-Si	Organic semiconductors
Carrier mobility [$cm^2 V^{-1} s^{-1}$]	1 to 100	1 max	50 to 100	0.1-10
Switching [$V dec^{-1}$][a)]	0.1 to 0.6	0.4 to 0.5	0.2 to 0.3	0.1-1.0
Leakage current [A][a)]	10^{-13}	~10^{-12}	~10^{-12}	~10^{-12}
Manufacturing cost	Low	Low	High	Low
Long term TFT reliability	High (forecast)	Low	High	Low in air
Yield	High	High	Medium	High
Process temperature [°C]	RT to 350	~250	<500	RT

[a)]Highly dependent on dielectric.

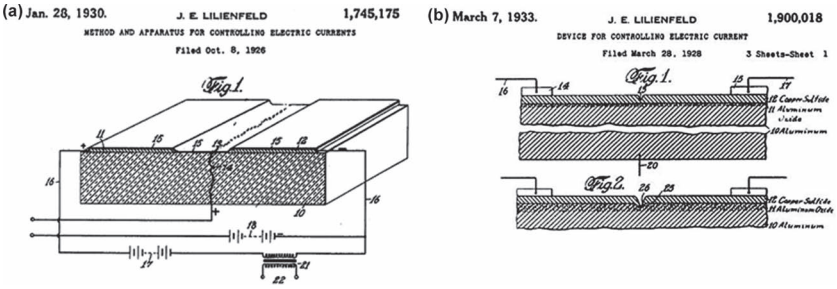


Figure 2. Initial patents of field-effect devices submitted by Lilienfeld: a) MESFET;[21] b) MISFET.[23]

semiconductor and a silicon monoxide insulator, using shadow masks to define the patterns of these layers. He used thin films of polycrystalline CdS semiconductor, similar to those developed for photodetectors, deposited onto glass substrates. In one pump down of his vacuum system, he would deposit a gold source and drain, then deposit polycrystalline semiconductor material over that and, finally, place a gate on top. This was a coplanar process that was similar to what he used in the tricolor vidicon. It should be noted that Weimer's work depended on depositions, not photoresists, which were used in developing integrated circuits, just then getting under way. At first, these deposited transistors weren't very good. But then he placed an insulator between the gate and the semiconductor material and got what he called "beautiful characteristics". His 1962 paper, *"The TFT — A New Thin-Film Transistor"*, in the Proceedings of the IEEE drew worldwide attention.[27]

Weimer used cadmium sulfide as the semiconductor material because it was a high-resistivity semiconductor with which he was somewhat familiar. Moreover, this was a pre-requirement to allow the conductance modulation via induced charges through the insulator layer. He later used cadmium selenide. This made for an even better field-effect transistor, not as good as silicon, Weimer recalls, but quite respectable.

Figure 3 shows the cross sectional and top views, output characteristics and a picture of a 1-in square glass plate (mounted on a lucite block) upon which three transistors have been evaporated.

Although the birth of transparent electronics is normally associated with reports on ZnO TFTs presented in 2001-2003, there were some tentative applications of oxide semiconductors as channel layers in TFTs forty years before, almost coincident with the initial CdS TFTs reported by Weimer in 1961. In fact, back in 1964, Klasens and Koelmans[8] proposed a TFT comprising an evaporated SnO_2 semiconductor on glass, with aluminium source-drain and gate electrodes and an anodized Al_2O_3 gate dielectric. Few details regarding electrical performance are provided and the transparent semiconductor is essentially used to demonstrate a new self-aligned lift-off process, where the SnO_2 layer allows to expose the photoresist to UV light penetrating from the bottom of the structure in all the areas expect the one

the thickness specified for the insulating layer was 100 nm, which is very similar to the one used nowadays in TFTs.[26] As it is normal with many innovations at that time, its practical realization was delayed until adequate materials and technologies were available for its fabrication. We can even say (and for most of us it could be surprising) that the TFT was the first solid-state amplifier ever patented.

It took one more decade for the first TFT to be produced. This was achieved by Weimer at the RCA Laboratories in 1962.[27–29] Weimer used a vacuum technique (evaporation) to deposit gold electrodes, a polycrystalline cadmium sulfide (CdS) n-type

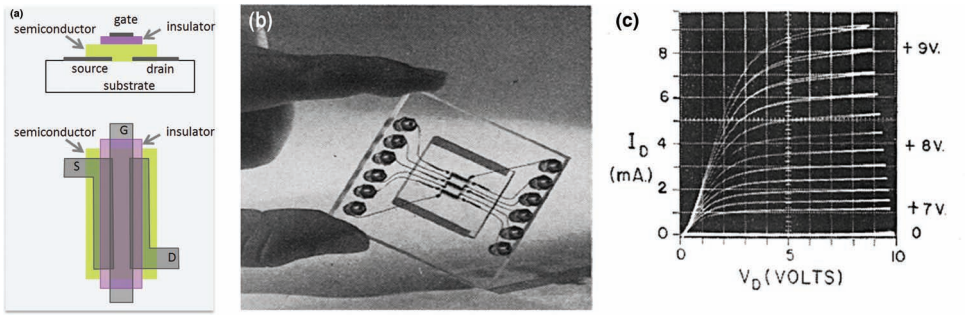


Figure 3. a) Cross-sectional view and top view, b) A 1-in square glass plate (mounted on a lucite block) upon which 3 TFTs have been deposited and c) Output characteristics of CdS TFTs reported by Weimer (adapted from [27]).

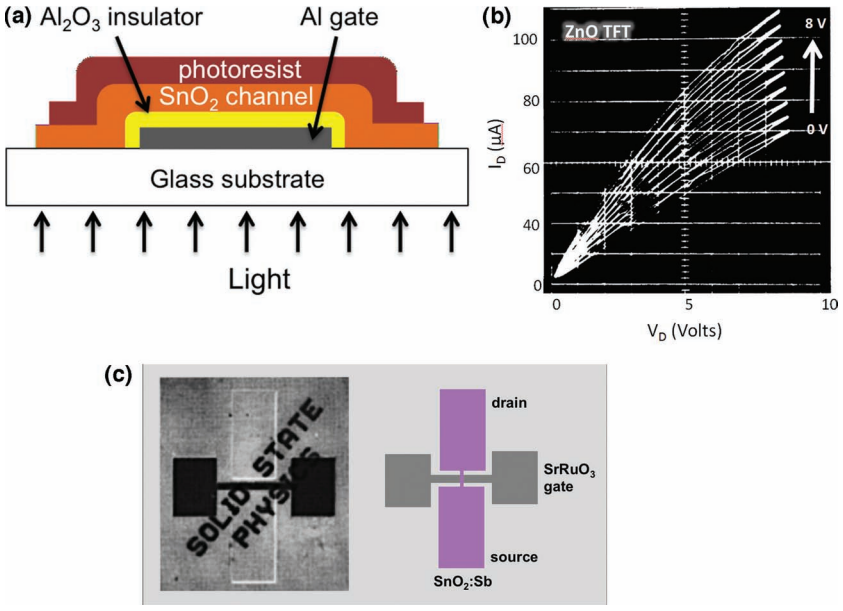


Figure 4. Initial TFTs employing oxide semiconductors as channel layers: a) Schematic of the SnO_2 TFT reported by Klasens and Koelmans in 1964, to show a new self-aligned lift-off process;[30]] b) Source-drain voltage-current characteristic of a single crystal ZnO FET, c) Picture and layout of the ferroelectric Sb:SnO_2 TFT proposed by Prins et al. in 1996.[31]

shielded by the aluminium gate electrode, defining this way the pattern of the source-drain electrodes (**Figure 4**a). In 1968, Boesen and Jacobs[9] reported a TFT with a lithium-doped ZnO single crystal semiconductor, with evaporated SiO_x dielectric and aluminium electrodes, but a very small drain current (I_D) modulation by applying a gate voltage (V_G) and no I_D saturation were observed on these devices (Figure 4b).

Aoki and Sasakura[32] obtained similar poor electrical performance in SnO_2 TFTs in 1970. Only in 1996 oxide semiconductors reappeared as channel layers, with two reports on ferroelectric field-effect devices employing SnO_2:Sb and In_2O_3, by Prins et al. and Seager, respectively.[31,33] Given that the main intent of the authors was to demonstrate hysteresis associated with the ferroelectric behaviour, little information is provided on these papers about device performance, but Prins and coworkers, for instance, report a low on/off ratio of 60. Still, it is noteworthy to observe that full transparency is for the first time persuaded in a TFT and it is only severely affected by the $SrRuO_3$ gate electrode (Figure 4c), although the authors mention that they also fabricated a fully transparent TFT by using a heavily doped SnO_2 gate electrode.

But good performing devices showing that oxide semiconductor-based TFTs could be a viable technology only started to appear in 2003, with the reports on ZnO TFTs by Hoffman et al, Carcia et al.and Masuda et al.[11,12,34] Hoffman and Carcia reported fully transparent devices (comprising TCO-based electrodes), already allowing to obtain respectable performance, comparable and even surpassing in some aspects the one typically exhibited by a-Si:H and organic TFTs, mostly in terms of mobility, which could be as high as 2.5 $cm^2\ V^{-1}\ s^{-1}$. However, the processing or post-processing temperatures of the semiconductor necessary to obtain good devices were still quite high, between 450-600 °C. But the work from Carcia et al. showed that using r.f. magnetron sputtering to deposit ZnO, similar electrical properties could be achieved with room-temperature processing of the semiconductor layer, even if on this case fully transparent structures were not demonstrated. After 2004 several reports continued to appear on oxide semiconductor-based TFTs, bringing different innovations to this emerging area. Some of the most important achievements were: ZnO TFTs exhibiting improved device performance (mainly regarding mobility) while keeping low or even room temperature ZnO processing;[35–37] non-vacuum processes to produce the ZnO layers;[38] first simulations of ZnO TFTs assuming that their properties are largely dictated by the polycrystalline nature of ZnO;[39] new methods for extraction of mobility in ZnO TFTs;[40] fully transparent ZnO TFTs produced at room temperature;[13] application of ZnO TFTs as UV photodetectors;[41,42] exploration of SnO_2 TFTs[43] and use of In_2O_3 or ZnO nanowires as channel layers.[25,44–46]

While most of the research work was being devoted to binary oxides such as ZnO, In_2O_3 or SnO_2, Nomura et al. suggested in 2003 to use a complex $InGaO_3(ZnO)_5$ (or GIZO) single-crystalline semiconductor layer in a TFT.[47] This layer was epitaxially grown on an yttria-stabilized zirconia substrate and allowed to obtain an impressive effective mobility of 80 $cm^2\ V^{-1}\ s^{-1}$, turn-on voltage of –0.5 V and on/off ratio of 10^6. Even if a very high temperature of 1400 °C was necessary to attain this level of performance, this paper made history, since it proves that high-performance oxide semiconductor-based TFTs are a reality. And in fact, in the following year Nomura et al. presented a work that definitely evidenced the enormous potential of oxide semiconductors (and multicomponent oxides in particular) for TFT applications, by demonstrating a transparent TFT on a flexible substrate using near-room temperature processing (**Figure 5**).[10] For this end, they used a PLD deposited amorphous GIZO layer as the semiconductor. Even if the performance was far from the single-crystalline TFTs presented by the same authors, a saturation mobility of 9 $cm^2\ V^{-1}\ s^{-1}$, threshold voltage of 1–2 V and on/off ratio of 10^3 could still be achieved, mostly because the low sensitivity of these multicomponent oxides to structural disorder.

Nomura's work opened the door for an impressively growing number of publications in the next years (see Figure 10 related to the evolution of papers published per year in this topic) regarding the application of amorphous multicomponent oxides as channel layers in TFTs. Several combinations of cations with $(n\text{-}1)d^{10}ns^0$ ($n \geq 4$) electronic configuration[4] started to be used for this end, being ZTO,[48–51] IZO,[52–55] and GIZO[6,56–60] the most widely explored ones. With the continuous improvements verified on these devices, it is now common to obtain remarkable electrical properties, considerably superior to a-Si:H[61] or organic TFTs, such as mobilities above 10 $cm^2\ V^{-1}\ s^{-1}$, turn-on voltages close to 0 V, on/off ratio exceeding 10^7 and subthreshold swing of 0.20 V dec^{-1}, with the indium-based semiconductors

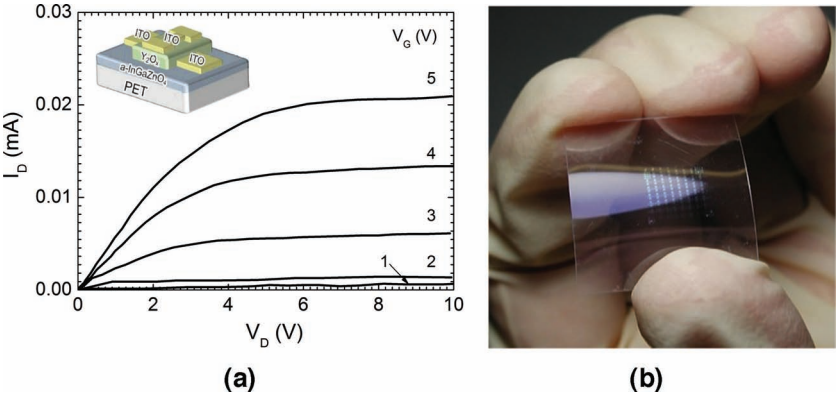


Figure 5. a) I_D. V_D characteristics of a flexible substrate with transparent a-GIZO TFTs; Photograph of the flexible TFT sheet bent at R = 30 mm presented by Nomura et al. in 2004 (adapted from [10]).

having the added advantage of allowing for very low or even room temperature processing. In fact, nowadays the processing temperature of these TFTs is dictated not by the semiconductor layer, but rather by the dielectric. Furthermore, it is important to note that if flexible and fully transparent TFTs are envisaged, the optimization of highly conducting TCOs deposited near room temperature for application as source, drain and gate electrodes is also a crucial requirement.[62–65]

Another important aspect deals with dielectric materials. Besides the huge development made on oxide semiconductors the dielectric has been somehow forgotten or, at least, left on a second plane, despite being as important as the channel layer on a TFT as its properties determines the charge accumulation at the dielectric/semiconductor interface. However, the existence of defects at the interface, as well as within the dielectric itself limits to a large extent the device's static and dynamic performance and reliability, on parameters such as mobility, leakage current, and photo-stability under electrical stress. This last topic is critical, nevertheless it is not explored in detail in this review, as there is not yet a consensus about the origin of this instability. It is known that the photoreliability of oxide TFTs is mostly deteriorated by negative rather than by positive bias stress. Several degradation models have been proposed, including the trapping of photogenerated hole carriers,[66,67] the creation of ionized oxygen vacancies[68] and the photodesorption of oxygen molecules.[69] In addition, the photoreliability is affected by a large number of parameters such as device structure/layout, semiconductor/dielectric material composition, passivation, among others, which limits a detailed analysis. A dedicated review on photo-stability should be taken into consideration in the future.

Based on all this, it seems that oxide semiconductors provide a solid and viable alternative for the present and future of TFTs, covering important drawbacks of the existing technologies, being a very attractive technology that allows for transparent, low cost, low temperature and high performance devices.

Figure 6 shows a schematic of the main landmarks achieved with either generic TFTs or oxide based TFTs.

3. Device Structure and Operation

TFTs are three terminal field-effect devices, whose working principle relies on the modulation of the current flowing in a semiconductor placed between two electrodes (source and drain). A dielectric layer is inserted between the semiconductor and a transversal electrode (gate), being the current modulation achieved by the capacitive injection of carriers close to the dielectric/semiconductor interface, known as field effect.[26]

Figure 7 shows the most common TFT structures. Depending if the source-drain are on opposite sides or on the same side of the semiconductor, the structures are identified as staggered and coplanar according to Weimer's definition.[70] Inside these, top- and bottom-gate structures exist, depending on whether the gate electrode is on top or bottom of the structure.

Each of these structures presents advantages/disadvantages, largely dictated by the materials used to fabricate the TFTs. For instance, the staggered bottom-gate configuration is widely used for the fabrication of a-Si:H TFTs, due to easier processing and enhanced electrical properties. As a-Si:H is light sensitive, the usage of this configuration is advantageous for the application of these TFTs in LCDs, since the metal gate electrode shields the semiconductor material from the effect of the backlight present on these displays. On the other hand, a coplanar top-gate structure is normally preferred for poly-Si TFTs. This is mostly attributed to the fact that the crystallization process of the semiconductor material generally requires high temperatures that could degrade the properties of other materials (and their interfaces) previously deposited, being favoured if the semiconductor is a flat and continuous film without any layers beneath it. Furthermore, the fact that in bottom-gate structures (both staggered and coplanar) the semiconductor surface is exposed to air can bring undesirable instability effects but can also be explored as a way to easily modify its properties, for instance by the facilitated adsorption of impurities during annealing or plasma treatments in a suitable atmosphere.

The schematics in Figure 7 only show the fundamental layers of a TFT, but other layers can also be introduced for different purposes. As an example, in silicon technology it is common to use highly doped semiconductor layers at the source-drain

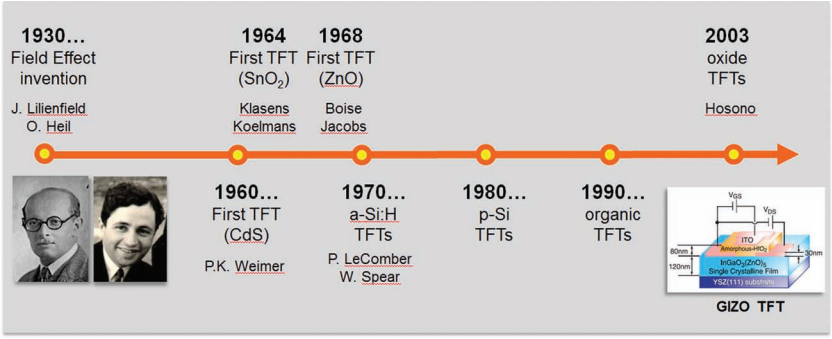


Figure 6. Main landmarks achieved with TFTs.

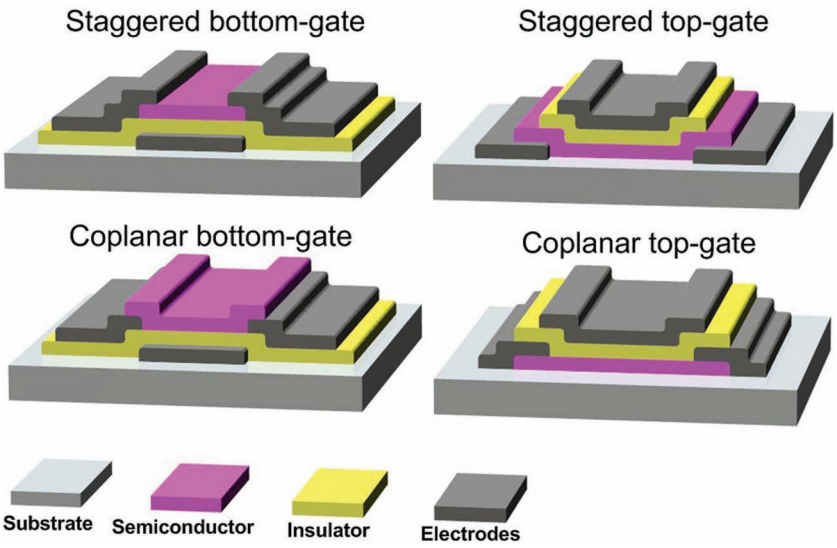


Figure 7. Schematics showing some of the most conventional TFT structures, according to the position of the gate electrode and to the distribution of the electrodes relatively to the semiconductor.

regions, in order to form low-resistance contacts. Also, an insulating film is often deposited on top of the semiconductor layer in staggered bottom-gate structures. This can allow for more accurate etching of the source-drain electrodes, without damaging the semiconductor surface, i.e. act as an etch-stopper.[71,72] This insulating layer can also have interesting effects on semiconductor films that strongly interact with environmental species such as oxygen or moisture, which is reflected in large variations of the electrical properties exhibited by the TFTs. This is particularly relevant for some of the first semiconductors used in TFTs, such as CdSe, and also for oxide semiconductors. Additionally, the insulating layer on top of the TFT structure can work as an effective mechanical and chemical protection of the devices from subsequent processes, such as their integration with liquid crystal cells.[73]

TFTs are quite similar to other field-effect devices in terms of operation and composing layers, such as the well-known MOSFETs used in high performance applications such as microprocessors or memories. However, important differences exist between these devices, some of them readily seen by inspecting their typical structures (**Figure 8**). First, while TFTs use an insulating substrate, normally glass, in MOSFETs the silicon wafer acts both as the substrate and the semiconductor. Thus, higher performance naturally arises for MOSFETs, given that the electrons flow in a single crystalline semiconductor, rather than in a polycrystalline or amorphous one. Also, the temperatures involved in the fabrication of both devices are quite different: while processing temperatures exceeding 1000 °C are common for MOSFETs, for instance to create the dielectric layer, in TFTs they are limited by parameters such as the softening point of the substrate, which for most common glass substrates does not exceed 600–650 °C.[71] In addition, MOSFETs have p-n junctions at the source-drain regions, which are absent in TFTs. This is related with another important difference in device operation: even if both TFTs and MOSFETs rely on the field effect to modulate the conductance of the semiconductor close to its interface with the dielectric, in TFTs this is achieved by an accumulation layer, while in MOSFETs an inversion region has to be formed close to that interface, i.e., a n-type conductive layer is created in a p-type silicon substrate.

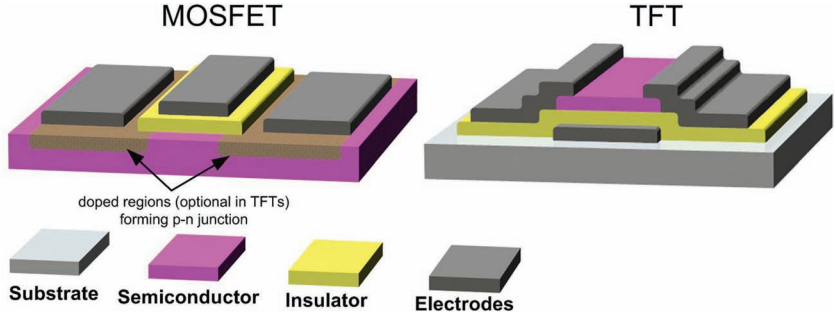


Figure 8. Comparison between the typical structures of MOSFETs and TFTs.

The most important TFT static characteristics are extracted from the output and transfer characteristics shown in **Figure 9**a and b, respectively and are: mobility (μ), on/off ratio, turn-on voltage (V_{ON}) and subthreshold swing (S).

On/off ratio: This is simply defined as the ratio of the maximum to the minimum I_D. The minimum I_D is generally given by the noise level of the measurement equipment or by the gate leakage current (I_G), while the maximum I_D depends on the semiconductor material itself and on the effectiveness of capacitive injection by the field effect. On/off above 10^6 are typically obtained in TFTs and a large value is required for their successful usage as electronic switches;[74]

V_T/V_{ON}: V_T corresponds to the V_G for which an accumulation layer or conductive channel is formed close to the dielectric/semiconductor interface, between the source and drain electrodes (channel region). For an n-type TFT, depending upon whether V_T is positive or negative, the devices are designated as enhancement or depletion mode, respectively. Both types are useful for circuit fabrication, but generally enhancement mode is preferable, because no V_G is required to turn off the transistor, simplifying the circuit design and minimizing power dissipation.[11] V_T can be determined using different methodologies, such as linear extrapolation of the I_D-V_G plot (for low V_D) or of the $I_D^{1/2}$-V_G plot (for high V_D), V_G corresponding to a specific I_D, ratio of conductance and transconductance, among others.[75] Even if considering only one methodology, large ambiguity can arise on the determination of V_T (for instance, by using different parameters in the linear fittings). The concept of V_{ON} is largely used in literature, simply corresponding to the V_G at which I_D starts to increase as seen in a log

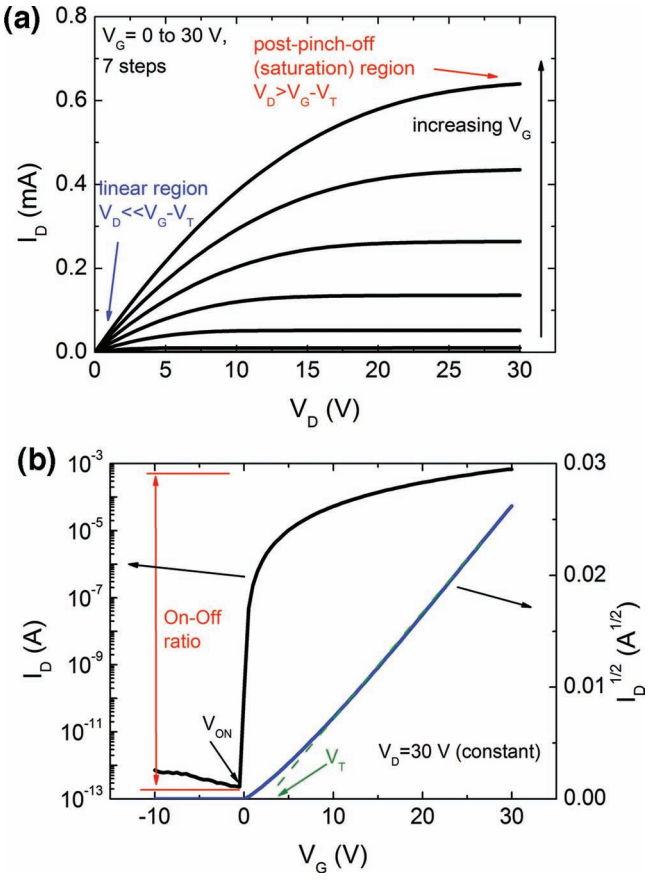


Figure 9. Typical a) output and b) transfer characteristics of a n-type oxide TFT.

I_D–V_G plot, or in other words, the V_G necessary to fully turn-off the transistor.[40]

Subthreshold swing (S): The inverse of the maximum slope of the transfer characteristic, it indicates the necessary V_G to increase I_D by one decade:

$$S = \left(\frac{d\log(I_D)}{dV_G}\bigg|_{\max} \right)^{-1} \quad (1)$$

Typically, S << 1, around 0.10–0.30 V dec^{-1} and small values result in higher speeds and lower power consumption.[74]

Mobility (μ): This is related with the efficiency of carrier transport in a material, affecting directly the maximum I_D and operating frequency of devices.[76] In a material, μ is affected by several scattering mechanisms, such as lattice vibrations, ionized impurities, grain boundaries and other structural defects.[76,77] On a TFT, since the movement of carriers is constrained to a narrow region close to the dielectric/semiconductor interface, additional sources of scattering should be considered, such as Coulomb scattering from dielectric charges and from interface states or surface roughness scattering.[77] Still, note that in a TFT μ is modulated by V_G, so scattering mechanisms become less relevant for particular bias conditions. Mobility of a TFT can be extracted using different methodologies. Following Schroder's nomenclature, one may have:[77]

Effective mobility (μ_{eff}): Obtained by the conductance (g_d) with low V_D:

$$\mu_{eff} = \frac{g_d}{C_i \frac{W}{L}(V_G - V_T)} \quad (2)$$

Field-effect mobility (μ_{FE}): Obtained by the transconductance (g_m) with low V_D:

$$\mu_{EF} = \frac{g_m}{C_i \frac{W}{L} V_D} \quad (3)$$

Saturation mobility (μ_{sat}): Obtained by the transconductance with high V_D:

$$\mu_{sat} = \frac{\left(\frac{d\sqrt{I_D}}{dV_G}\right)^2}{\frac{1}{2}C_i \frac{W}{L}} \quad (4)$$

Each methodology has its advantages and drawbacks. Even if μ_{eff} includes the important effect of V_G, it requires the determination of V_T and is more sensitive to contact resistance (low V_D). This last issue is also verified for μ_{FE}, but μ_{FE} does not require V_T and is easily calculated by the derivative of transfer characteristics, consequently it is a widely used parameter. Finally, μ_{SAT} does not require V_T and is less sensitive to contact resistance. However, it describes a situation where the channel is pinched-off, i.e., its effective length is smaller than L, which is intrinsically not assumed by the classical model.[26]

Other methodologies can be found in literature, such as the average (μ_{avg}) and incremental (μ_{inc}) mobility proposed by Hoffman.[40] While the former provides an average value of all the carriers induced in the channel, the latter probes the mobility of carriers as they are incrementally added to the channel, providing valuable insights into carrier transport.

In most manuscripts only a peak value of μ_{eff}, μ_{FE} or μ_{sat} is presented. However, by plotting Equations 2, 3 or 4 as a function of V_G allows for a more complete understanding of the device physics, clearly showing effects such as mobility degradation due to contact resistance or increased interface scattering as V_G increases.

4. Recent Progress of n-Type Oxide TFTs

4.1. Historical Overview

The large number of research groups that are now working on transparent electronics have produced more than 541 papers between 2001 and 2010, which limits a precise and detailed analysis of the work. In order to have an idea about the scientific output in terms of papers produced, in the graphic of **Figure 10** we show the evolution of published papers between 2001 and 2010 only related to n-type oxide based TFTs. The bar chart is divided into three main categories function of the semiconductor channel layer: ZnO, GIZO and others including ZTO, ITO, IZO, IZTO, IGO and IHZO.

From the bar chart it is interesting to point out the sharp increase of publications appearing after 2006, reaching a total of 161 in 2009. In 2010 it was observed a small decrease

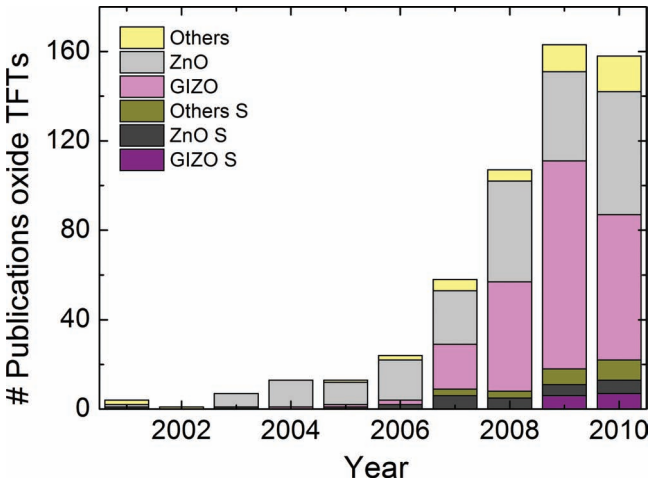


Figure 10. Number of oxide TFTs related papers published per year. In the legend S means "solution processed" (data compiled from refs. [66,78–276] only dealing with GIZO TFTs, the ones corresponding to solution process are in Tables 2a, b and c.

concerning the number of GIZO TFTs publications, but this could be associated to the fact that we have now industries starting producing displays using this technology, which pushes the researchers to investigate new materials as well as new technologies. From the graphic it is also interesting to see the evolution for solution processed TFTs especially after 2009 (a detailed analysis will be given in the next section).

From the analysis of roughly 200 papers published on GIZO TFTs two aspects can be highlighted: first, the leading deposition technique is sputtering (more than 90%), and secondly it is possible to grow GIZO TFTs at temperatures lower than 150 °C with acceptable electrical performance. Besides the common part associated with the channel layer material, it is very hard to compare the TFT characteristics since, the type of substrate and structures used are different. In some cases the channel layer is not patterned, the dielectric material and the interface are different and depending on the specific layout used we can have the source/drain electrodes completely overlapping the channel layer.[277] All these technological/geometry aspects will affect the electrical properties of the TFTs limiting a real comparison of devices produced in different laboratories, specially the figure of merit: channel mobility. Besides that and since we do not want to repeat what is already published in some recent oxide based TFT reviews ([20,278,279]), we will present in this section a summary of the main achievements concerning n-type oxide TFTs. We have done an exhaustive survey at WOK from Thomson Reuters and have tried to include all the work published in this topic until the submission of this review (July 2011). If there is some work not included we would like to apologise the authors in advance. In the following paragraphs we will refer to the effect of chemical composition, electrical stability and passivation issues.

4.2. Effect of Oxide Semiconductor Composition

Starting with the effect of GIZO composition on the TFTs electrical properties, some work was already been reported by Iwasaki et al.[60] and by Barquinha et al.[6] While Iwasaki used a combinatorial co-sputtering study with 3 oxide targets (ZnO, Ga_2O_3 and In_2O_3), Barquinha et al. used specific GIZO target compositions. For this particular study the semiconductor layers were produced with an oxygen percentage of 0.4%, being the final devices annealed at T_A = 150 °C. The devices, with a staggered bottom gate configuration, were produced on silicon substrates with 100 nm thick PECVD SiO_2, using e-beam evaporated Ti-Au source/drain electrodes. Transfer characteristics are presented in **Figure 11** and **Figure 12** for binary/ternary and ternary/quaternary compounds, respectively, being the trends of μ_{FE} and V_{ON} with composition shown in **Figure 13**.

The analysis of the data denotes significant differences and trends. Starting by the TFTs comprising binary compounds, large differences are obtained for In_2O_3, ZnO and Ga_2O_3 devices. This is naturally related with the different electrical properties of the respective thin films. For these deposition conditions the carrier concentration (N) is ≈10^{18} cm^{-3} for In_2O_3, which renders the Fermi level (E_F) to be very close to the conduction band minimum (CBM), making it impossible to deplete the semiconductor with reasonable V_G values. Hence, even if a very large μ_{FE} is achieved for the In_2O_3 TFTs, due to the E_F pinning above CBM as V_G is increased, the devices are not usable as transistors, since they cannot be switched off. On the other hand, Ga_2O_3 films have very large resistivity ($\rho > 10^8$ Ω cm), presumably due to a very low N and large density of empty traps, in addition to the large bandgap, above 4 eV. This results in

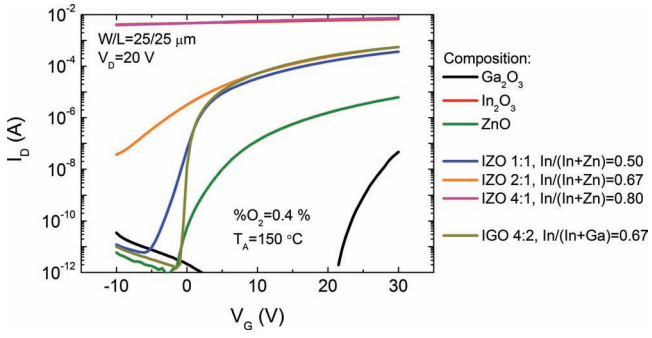


Figure 11. Effect of oxide semiconductor target composition on the transfer characteristics of TFTs annealed at 150 °C: binary and ternary compounds.

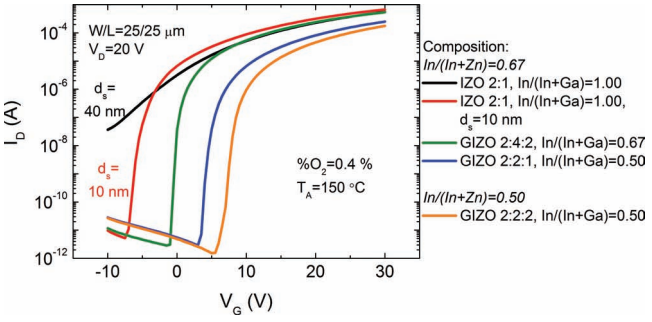


Figure 12. Effect of oxide semiconductor target composition on the transfer characteristics of TFTs annealed at 150 °C: ternary and quaternary compounds. The effect of decreasing d_s from 40 to 10 nm for IZO 2:1 is also shown.

very poor device performance, with $V_{ON} > 20$ V, $\mu_{FE} \approx 0.02$ cm^2 V^{-1} s^{-1} and large ΔV_{ON}, above 6 V (ΔV_{ON} is the shift of V_{ON} after measuring the transfer characteristics three consecutive times, giving a fast indication of how stable the transistors are), which is not improved even for T_A = 500 °C. Matsuzaki et al. also reported similar characteristics for Ga_2O_3 TFTs, with $\mu_{inc} \approx$ 0.05 cm^2 V^{-1} s^{-1} and $V_{ON} > 10$ V for T_A = 500 °C.[280] ZnO seems to be the best binary compound for oxide TFT application, at least considering the range of deposition conditions used herein. In fact, close to 0 V_{ON}, *on/off* exceeding 10^6 and $\Delta V_{ON} \approx$ 1 V are achieved on these ZnO TFTs. Still, the small slope of the transfer characteristics is synonym of a relatively high S (0.90 V dec^{-1}) and the low maximum I_D is indicative of a low μ_{FE} (1.6 cm^2 V^{-1} s^{-1}). Two reasons can be pointed as the main justification for the moderate performance of the ZnO TFTs: first, $\rho \approx 10^7$ Ω cm, which is indicative of low N and/or large unfilled trap densities; second, the existence of grain boundaries, which are associated with depletion regions with high potential barriers that greatly affect the movement of free carriers.

Multicomponent amorphous oxides, in general, allow for considerably better TFT performance than binary compounds. Rather than having carrier transport limited by grain boundaries, in amorphous oxides carrier transport is mostly dictated by the potential barriers located around the CBM, associated with the structural randomness, which can easily be surpassed in properly processed films by increasing V_G. Furthermore, the relative proportion of the cations directly controls the background N within a broad range, which has direct implications on transistor performance. For IZO TFTs with In/(In + Zn) atomic ratios between 0.50 and 0.80 it is verified that the properties tend to get closer to the predominant binary compound, i.e., for In/(In + Zn) = 0.80 both I_D and μ_{FE} are similar to In_2O_3 TFTs, while for In/(In + Zn) = 0.50 the properties start to move away from those of In_2O_3 TFTs toward the ones of ZnO TFTs. Intermediate properties are obtained for In/(In + Zn) = 0.67. This means that N and μ_{FE} get higher for increased indium content, but only the IZO 1:1 TFTs are able to present clear *on*- and *off*-states within the V_G range used here. Considerably better device performance is achieved using IGO[281] instead of IZO. This arises as a direct consequence of the strong bonds that gallium forms with oxygen,[282] suppressing the generation of free carriers and raising ρ relatively to IZO films. In fact, besides other important drawbacks of IZO such as increased light sensitivity, the difficulty in controlling the background N down to low values (at least <10^{16} cm^{-3}) in IZO makes researchers (and industry) move for materials such as GIZO to fabricate the active layers of TFTs. Still, note that the problem of high background N can be attenuated by decreasing the semiconductor thickness (d_s): for instance, by using IZO 2:1 d_s = 10 nm rather than the "standard" 40 nm used for the oxide TFTs presented throughout this paper, the transistors can be fully switched-off for V_G <–7 V. This is justified by the fact that the depletion region created at the back (i.e., air exposed) surface of the active layer due to the interaction with environmental oxygen can be extended to the semiconductor/dielectric interface when a low d_s is used.[283]

The effect of adding different amounts of gallium to IZO is shown in Figure 12. Given the stronger bonds of gallium with oxygen, background N decreases as gallium content in GIZO increases, resulting in a considerable shift of V_{ON} toward more positive values. This is naturally advantageous for large In/(In + Zn), since it permits the production of TFTs that clearly switch between *off*- and *on*-states. However, for smaller In/(In + Zn), gallium incorporation can also lead to devices with considerably lower μ_{FE} and higher V_{ON} and ΔV_{ON}. This can be seen by comparing GIZO 2:4:2 with 2:2:1 and 2:2:2 compositions and is explained by the larger fraction of empty traps that need to be filled before E_F reaches CBM or above it for materials with lower background N. Additionally, since the ratio of In/(In + Zn + Ga) starts to decrease, the higher structural disorder close to CBM increases the potential barriers that constrain the movement of free carriers, making the E_F shifting above CBM harder, as mentioned in the previous point. The trends verified for In/(In + Zn) in Figure 11 can also be observed in Figure 12, for fixed In/(In + Ga) atomic ratios (compare GIZO 2:2:1 with 2:2:2), although to a smaller extend than in gallium-free

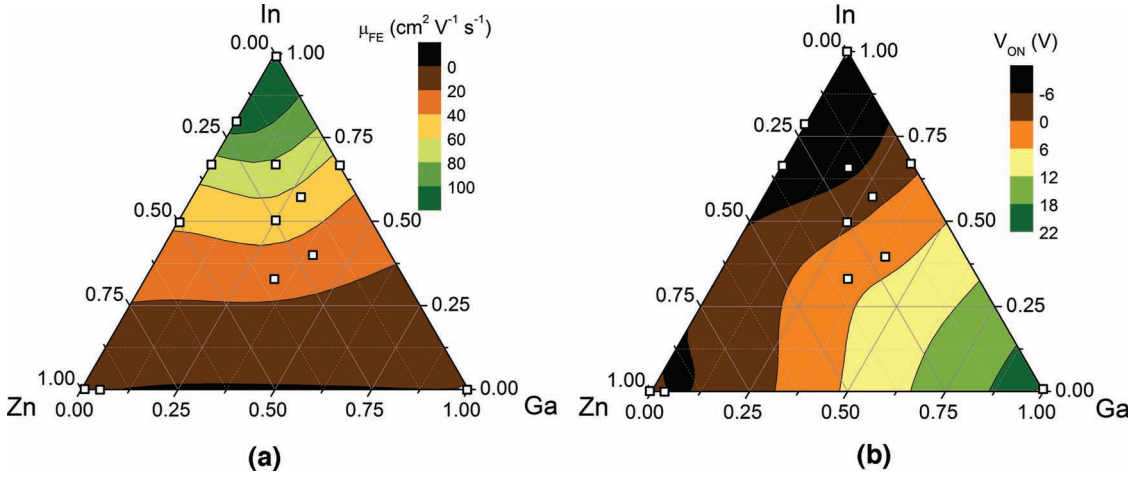


Figure 13. a) μ_{FE} and b) V_{ON} obtained for TFTs with different oxide semiconductor compositions, in the gallium-indium-zinc oxide system. Devices annealed at 150 °C, with%O_2 = 0.4%.

materials, since the properties start to be essentially dominated by the gallium content when this element is present.

Naturally, all the compositional effects also depend on the remaining processing parameters and so the specific results presented here for a particular composition should not be taken as an entirely strict rule: in fact, a large number of reports regarding stable TFTs with close to 0 V_{ON} exist in the literature, for compositions around 2:2:2 and 2:2:1.[72,284,285] Nevertheless, the overall trends verified here for IZO[286–288] and GIZO[58,60,289–291] devices were also verified by other authors.

Despite that the increase of V_G above V_{ON} leads invariably to the enhancement of μ_{FE}, as predicted by conventional field-effect theory, the transconductance (hence μ_{FE}) is changed in different ways, depending on the composition and structure of the oxide semiconductor material. **Figure 14** illustrates this for GIZO 2:4:2 (amorphous) and ZnO (polycrystalline) TFTs, both having semiconductor layers deposited with $\%O_2 = 0.4\%$ and subjected to $T_A = 150$ °C. Given that the PECVD SiO_2 has a high breakdown voltage, the V_G range is extended for both cases in order to see all the μ_{FE}–V_G regimes.

For the GIZO TFT (Figure 14a) an almost abrupt increase of μ_{FE} is verified after V_{ON}, given the small S. Physically, E_F is raised very quickly above CBM by V_G, since the trap density is very low and very large μ_{FE} can be achieved when the small potential barriers associated with structural disorder are surpassed, which happens for $V_G \approx 20$–30 V, where μ_{FE} is maximum. As V_G gets higher than these values, the conductive channel is drawn closer to the GIZO/SiO_2 interface, which contributes to increased scattering effects of the large density of induced charges, resulting in a decrease of μ_{FE}.[26] An electron injection barrier at the source electrode may also contribute for this drop in μ_{FE}, as proposed by Dehuff et al.[52] A considerably different μ_{FE}–V_G trend is observed for the ZnO TFT (Figure 14b). For this case the increase of μ_{FE} with V_G occurs gradually, essentially due to the polycrystalline structure of ZnO with small grain sizes, hence large density of grain boundaries. Some models describe quite well the behaviour of polycrystalline TFTs, namely the one proposed by Levinson in 1982[292] and more recently the one of Hossain, specifically oriented for ZnO TFTs.[39] From these models it can be seen that the barrier height associated with the depletion regions at the grain boundaries is modulated by the total N, which has contributions both from the background N and from the charges induced by V_G. Furthermore, for smaller grain sizes the width of the depletion regions can extend deep inside the crystallites and even overlap with adjacent depletion regions, resulting in very high ρ. For the ZnO TFTs presented in Figure 14b) the modulation of these effects by V_G should be dominant and overshadow ZnO/SiO_2 interface scattering, even if V_G is increased up to 100 V. Although measured in a smaller V_G range, Nishii et al. also obtained a similar μ_{FE}–V_G trend in ZnO TFTs.[35] For a large V_G range, saturation (and even decreasing) of mobility is observed by Hoffman for $V_G > 70$ V, on ZnO TFTs produced on thermal SiO_2.[40] Still, note that mobility is extracted by Hoffman using a different methodology, designated by incremental mobility, which probes the mobility of carriers as they are incrementally added to the channel, rather than averaging the mobility of all the carriers present in the channel for a given V_G.[40] In fact, by using the more conventional "average mobility", physically similar to μ_{FE}, mobility saturation is not achieved in Hoffman's paper. By plotting μ_{inc}–V_G for the data depicted in Figure 14b, saturation is still not obtained, which can be due to different ZnO processing conditions (plausible given the considerably higher μ_{FE} achieved by Hoffman) and also to the effect of I_G that for the present PECVD SiO_2 starts to increase considerably for $V_G > 70$ V.

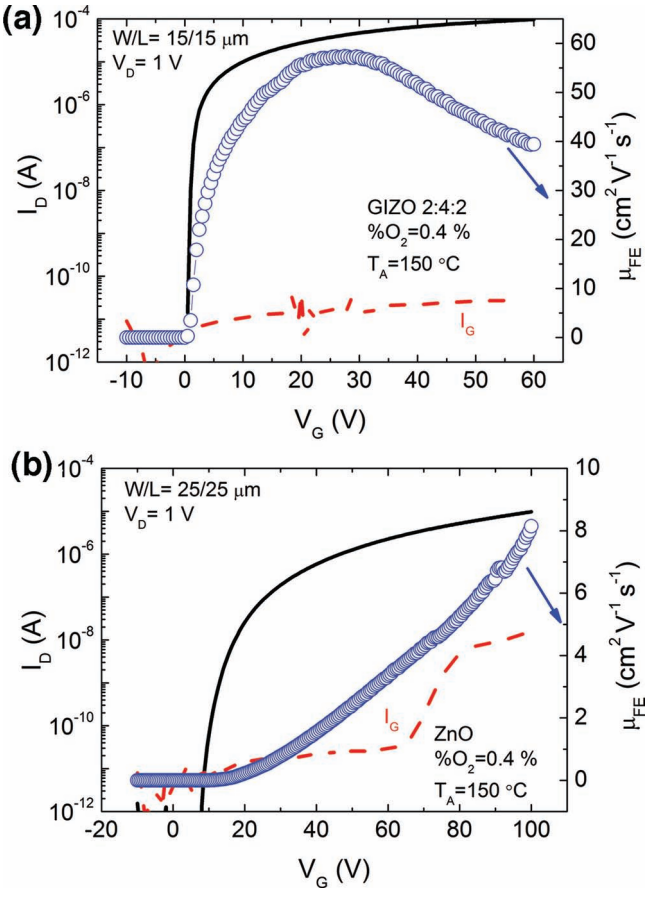


Figure 14. Transfer characteristics and μ_{FE}-V_G plots measured for high V_G for TFTs annealed at 150 °C, based on a) GIZO 2:4:2 and b) ZnO.

Some comments should also be made regarding the other polycrystalline binary compound, In_2O_3. If the devices employing this semiconductor are annealed at a higher T_A to allow for complete crystallization, such as $T_A = 300$ °C, intermediate properties to those observed in Figures 14a and b are observed. Although grain boundaries can still affect the movement of the free carriers, their effect should be considerably smaller, given the larger grain size and larger N of this material. Hence, in the unbiased state, most of the traps associated with grain boundaries can be compensated by the background N, leaving more of the V_G induced charges available to increase the transconductance.

4.3. Electrical Stress Measurements

Stress measurements are crucial to understand instability mechanisms on devices as well as to predict if the technology is suitable to be used in integrated circuits. Hence, the dependence of

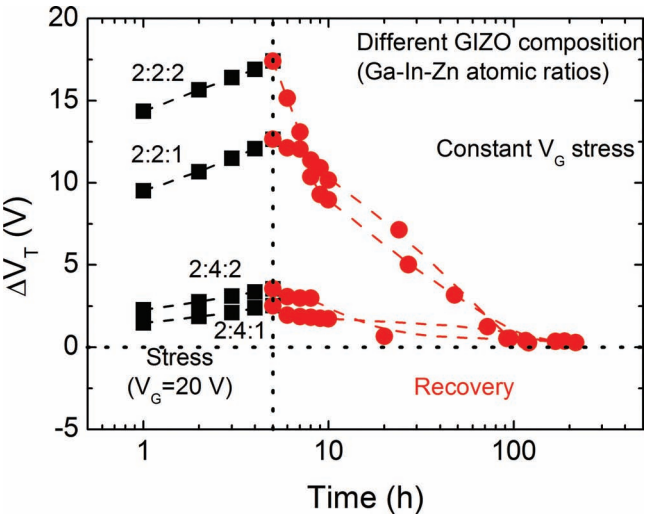


Figure 15. ΔV_T obtained on gate-bias stress measurements during 5h, for oxide TFTs with different GIZO compositions, annealed at 150 °C.

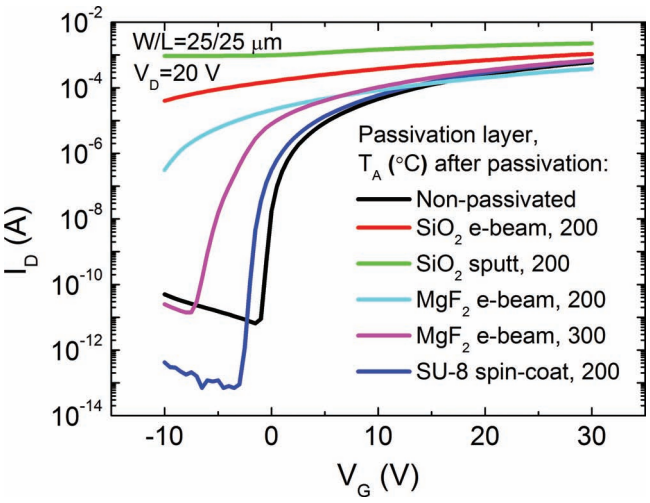


Figure 16. Transfer characteristics obtained for GIZO TFTs with different passivation layers (adapted from [277]).

GIZO composition on the electrical stability of oxide TFTs under gate-bias stress measurements was also studied, for GIZO layers with%O_2 = 0.4% and T_A = 150 °C (**Figure 15**). Stress measurements were carried out by applying a constant V_G = 20 V during 5 h, while keeping the source and drain electrodes grounded.

As happens with other semiconductor technologies,[293–295] reversible charge trapping at or close to the dielectric/semiconductor interface, resulting in a shift of V_T (ΔV_T), is the most frequent instability mechanism.[222,296–300] The same is verified here, with 2:2:2 and 2:2:1 GIZO compositions resulting in the most unstable devices, as would be predictable given the larger ΔV_{ON} and hysteresis verified for these compositions. As mentioned in 4.2, as the ratio of In/(In+Zn+Ga) starts to decrease, higher structural disorder appears close to the CBM, which can give rise to trap states that degrade the stability. Nevertheless, regardless of composition, the initial properties can be recovered some hours after stress without any subsequent annealing treatment, which is consistent with conventional charge trapping mechanisms rather than defect state creation or ionic drift.[30,299,301,302] Note that the devices analyzed to compose Figure 15 were fabricated by employing the oxide semiconductor deposition conditions yielding the most stable devices. If these conditions or other device materials (such as the dielectric layer) are changed, a subsequent annealing treatment might be required to recover the initial properties of the transistors.[277,303]

Despite GIZO 2:4:1 and 2:4:2 compositions provide the best performing and more stable transistors, device stability can be greatly improved using a passivation layer on top of GIZO. In fact, different authors reported both improved stability (e.g.[298,301,304,305]) and process yield (e.g.[107]) when using proper passivation layers on oxide TFTs.

4.4. Effect of Passivation Layer

Figure 16 shows the transfer characteristics obtained for GIZO TFTs having different passivation layers, deposited using different techniques: SiO_2 by e-beam evaporation and sputtering; MgF_2 by e-beam evaporation and SU-8 by spin-coating.

The results can be understood by investigating the effects occurring at the air-exposed surface of GIZO. In a non-passivated oxide semiconductor oxygen is physisorbed at the back surface, creating acceptor-like surface states that attract electrons from the semiconductor, giving rise to a depletion region in the semiconductor that can even extend from the air-exposed surface to the dielectric/semiconductor interface. If a passivation layer is placed on top of the air-exposed surface, oxygen adsorption is inhibited, and depending on the passivation material and its deposition technique, an accumulation layer can even be formed at the semiconductor/passivation interface for instance, if metal cation-oxygen bonds are broken during deposition[74,306,307] or if the passivation layer has a large density of positive charges. Based on this background, vacuum deposition techniques (e-beam and sputtering) result on the largest negative shifts of V_{ON} after passivation, since some oxygen from GIZO's back surface can be removed during pump down time. Additionally, the intense substrate bombardment occurring during sputtering can break weak metal cation-oxygen bonds, generating oxygen vacancies that increase *N*. This was in fact observed by different authors when exposing a GIZO surface to reactive ion etching (RIE) or to N_2 and NH_3 plasma treatments.[72,306,308] Hence, the biggest variations occurring after passivation are verified for sputtered SiO_2, then for e-beam SiO_2 and MgF_2. The effect of T_A = 300 °C is also shown for MgF_2, being possible to switch off the transistors for V_G < −7.5 V. Despite the largely negative V_{ON}, MgF_2 passivated devices also exhibit a negative shift of V_{ON} in consecutive transfer characteristics measurements, as well as counter clockwise hysteresis, suggesting that ionic drift mechanisms can be present in the device.[30,309,310]

SU-8, an epoxy-based negative chemically amplified resist that is commonly used for the fabrication of high aspect ratio features,[311] provides the best device performance. To a large extent, this can be justified by the non-vacuum deposition technique (spin-coating), without physical substrate bombardment.

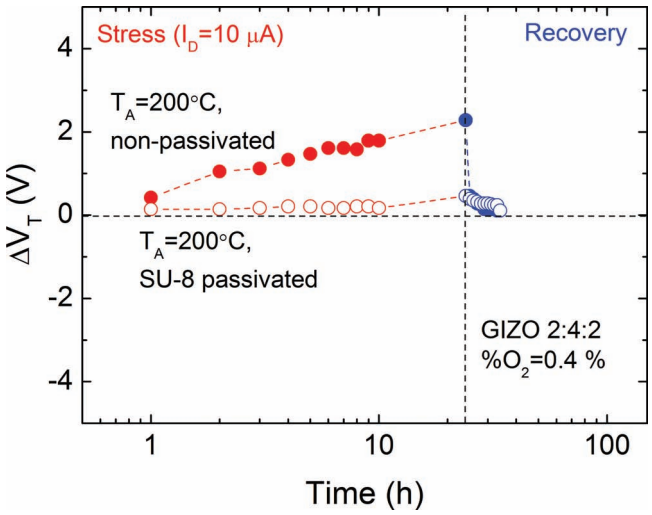


Figure 17. ΔV_T vs stress/recovery time obtained from constant I_D stress measurements of GIZO TFTs with and without SU-8 passivation,%O_2 = 0.4% and T_A = 200 °C (adapted from [312]).

Even if SU-8 passivated TFTs without a subsequent annealing process exhibit a large negative V_{ON} (≈ −10 V), the performance is significantly improved after T_A = 200 °C. At this stage, cross-linking of the SU-8 layer is fully achieved (confirmed by FTIR analysis) and remaining H^+ ions available at the passivation layer (due to the decomposition of the photoacid generator present in SU-8), close to its interface with GIZO, can probably capture some electrons from GIZO, re-establishing a depletion layer close to the back surface of GIZO.

SU-8 passivation also provides a remarkable improvement on the stability of the devices, as shown in **Figure 17**, where results for constant I_D stress measurements for passivated and non-passivated devices are plotted.

A small and recoverable ΔV_T = 0.46 V could be obtained after 24h of stress at I_D = 10 μA for the SU-8 passivated GIZO TFTs. The improvement over non-passivated devices should again be related with the GIZO's back surface, where a barrier is formed by the passivation layer, inhibiting oxygen adsorption/desorption processes that are known to be potentiated when ZnO-based materials are subjected to electric fields.[313] On the contrary, in non-passivated devices, oxygen can be adsorbed as the stress measurement progresses, widening the depletion layer close to the back surface and raising V_T. Improvements on the stability of passivated oxide TFTs are also reported in literature, for instance by Cho et al. and Levy et al.[298,304]

4.5. Effect of Dielectric Material

The stability and overall performance of a TFT also depend to a great extent on the dielectric layer. The results presented above refer to an optimized PECVD SiO_2 process at 400 °C, but if low-temperature electronics are envisaged, alternative dielectrics and/or processing techniques need to be used. Chemically deposited organic dielectrics are being investigated for oxide TFTs with very promising results, but generally their growing and/or curing process is slow and/or requires high temperatures.[314,315] Physical routes like sputtering are another possibility for low-temperature dielectric fabrication, but generally the low sputtering rates of dielectrics requires the usage of highly-energetic deposition processes (for instance, high power and/or low deposition pressure) that can negatively affect the growing films and their interfaces. Hence, materials with a high dielectric constant (high-κ) are preferable, given that the increased capacitance can compensate the higher density of interface traps, decreasing S and the operating voltage.[30] Still, most of the high-κ dielectrics present at least two issues that can degrade performance and stability of oxide TFTs: (i) hey exhibit a polycrystalline structure and a rough surface, which can contribute to reduced reliability, since grain boundaries act as preferential paths for impurities diffusion and leakage current, and degraded interface properties[30,316] and (ii) high-κ dielectrics generally have lower E_G and smaller band offsets relatively to the semiconductor than conventional SiO_2 or SiN_x:H, leading to a low breakdown voltage and high leakage current (I_G).[317]

Multicomponent and/or stack dielectrics, composed by mixtures of high-κ (e.g. Ta_2O_5 or HfO_2[318,319]) and high-E_G (e.g. SiO_2 or Al_2O_3) have been studied to solve these issues. Most of these materials can remain amorphous even at temperatures exceeding 500 °C, preserving an overall high-κ and improving the band offsets relatively to the semiconductor. Some relevant results regarding the integration of multicomponent/stack dielectric with oxide semiconductor technology are provided in ref[81].

At CENIMAT|I3N we have been studying both Ta- and Hf-based dielectrics for integration with GIZO TFTs. **Figure 18** shows transfer characteristics of GIZO TFTs employing sputtered SiO_2, Ta_2O_5 and co-sputtered Ta_2O_5-SiO_2 (denoted as TSiO) dielectrics, being the final devices annealed at 150 °C.[303] Sputtered SiO_2 results in poor overall device performance, with a low μ_{FE} (≈1 $cm^2 V^{-1} s^{-1}$) and high S (≈1 V dec^{-1}). Even if Ta_2O_5 can provide considerably improved performance, its low E_G and poor band offset relatively to GIZO result in a low yield/reproducibility and large off-currents. By using co-sputtered TSiO a

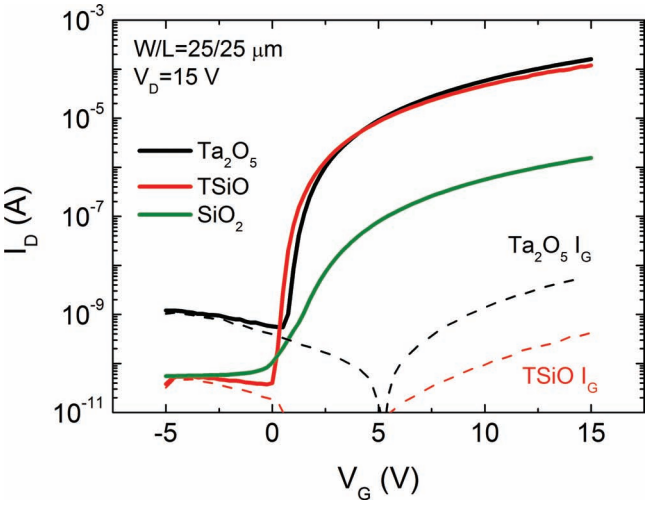


Figure 18. Transfer characteristics of GIZO TFTs using sputtered SiO_2, Ta_2O_5 and co-sputtered TSiO dielectrics. Devices annealed at 150 °C (adapted from [303]).

good compromise between the lower off-current of SiO_2 and lower S and higher μ_{FE} of Ta_2O_5 are obtained.

But even with TSiO, a narrow band offset is obtained with GIZO, making the reliability and reproducibility of GIZO TFTs using this dielectric an issue, being frequent to find in one substrate several devices with shorted-gates or, in less extreme cases, devices with large electrical properties variations, namely in their *off*-current. Hence, even if some TSiO-based TFTs can sustain repeated and severe stress tests, such as constant I_D = 10 μA during 24h,[303] multilayer dielectrics composed by TSiO stacked between two thin layers (≈20 nm) of SiO_2 (denoted by S-TS-S) are being investigated. Even if hysteresis is slightly increased for the multilayer structures when compared with TSiO (mostly due to the non-optimized SiO_2/GIZO interface), the reproducibility, reliability and overall transistor performance are significantly improved by using the multilayer structure (**Figure 19**). This is due to the fact that the material in contact with GIZO is now a high-E_G dielectric with a large conduction band offset with GIZO and also due the existence of discontinuities or interfaces between the different layers composing the dielectric that prevent the easy flowing of charges through the overall structure. For these devices, μ_{FE} = 12.7 cm^2 V^{-1} s^{-1}, V_{ON} = –0.4 V, *on/off* = 3 × 10^8 and S = 0.20 V dec^{-1} are obtained. The dominant instability mechanism on these devices appears to be charge trapping at or close to the dielectric/semiconductor interface, resulting in a reversible $\Delta V_T \approx$ 5 V after 12 h with I_D = 10 μA.

A multilayer approach was also used to improve the properties of Hf-based dielectrics. GIZO TFTs employing HfO_2 dielectric exhibit a sharp increase of I_G for V_G > 5 V (**Figure 20**a). The small range of usable V_G and lack of reliability/reproducibility of HfO_2-based TFTs might be associated with the higher bombardment effects during film growth (higher P_{rf} than Ta_2O_5), which can broaden the band-tails and decrease the band-offsets with GIZO, and also with the polycrystalline structure of sputtered HfO_2 films. But similarly to what was observed for tantalum-based dielectrics, a multilayer stack with a HfO_2-SiO_2 layer between two thin layers of SiO_2 (overall stack denoted by S-HS-S) results in considerably improved electrical properties, with a very low I_G that allows obtaining *on/off* exceeding 10^9. Besides that, S-HS-S-based TFTs exhibit μ_{FE} = 17.0 cm^2 V^{-1} s^{-1}, V_{ON} = 1.2 V and S = 0.22 V dec^{-1}. Although the ΔV_T under constant I_D stress measurements is higher than for transistors with S-TS-S, charge trapping is again the only significant instability mechanism verified, being the initial properties of the devices fully recoverable after 48h recovery time (Figure 20b).

An improvement of performance and stability of oxide TFTs with hafnium-based multilayer dielectrics was also verified by Chang et al. and Lee et al.,[219,320,321] by showing that ZnO TFTs employing an $Al_2O_3/HfO_2/Al_2O_3$ dielectric exhibit a considerable suppression of charge trapping, traduced in lower hysteresis and lower ΔV_T than similar TFTs with HfO_2.

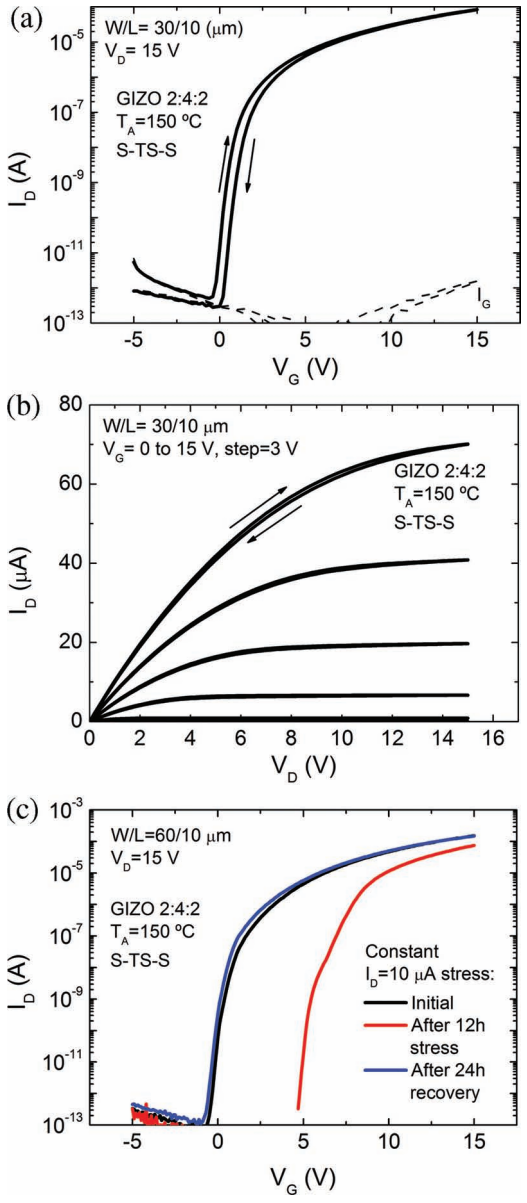


Figure 19. Electrical properties obtained for GIZO TFTs with S-TS-S dielectric: a) transfer characteristics; b) output characteristics; c) transfer characteristics evolution during constant I_D stress measurements. Devices annealed at 150 °C.

4.6. Solution-Based TFTs

Following Moore´s law the number of transistors per microelectronic chip has doubled every 18 months. Nevertheless the cost of a chip per unit of area has remained relatively static for the last three decades. This leads to the developing of new and inexpensive technologies, like for example printing technologies. Current methods for the production of functional inorganic electronic devices are based on the sequential deposition, patterning, and etching of selected semiconducting, conducting, and insulating materials. These sequential processes generally involve multiple photolithography and vacuum-deposition processes, which contribute to their high manufacturing costs. Direct printing of inorganic materials offers the possibility of depositing thin films using a direct additive patterning processes that enables the fabrication of high-performance and ultralow-cost electronics.

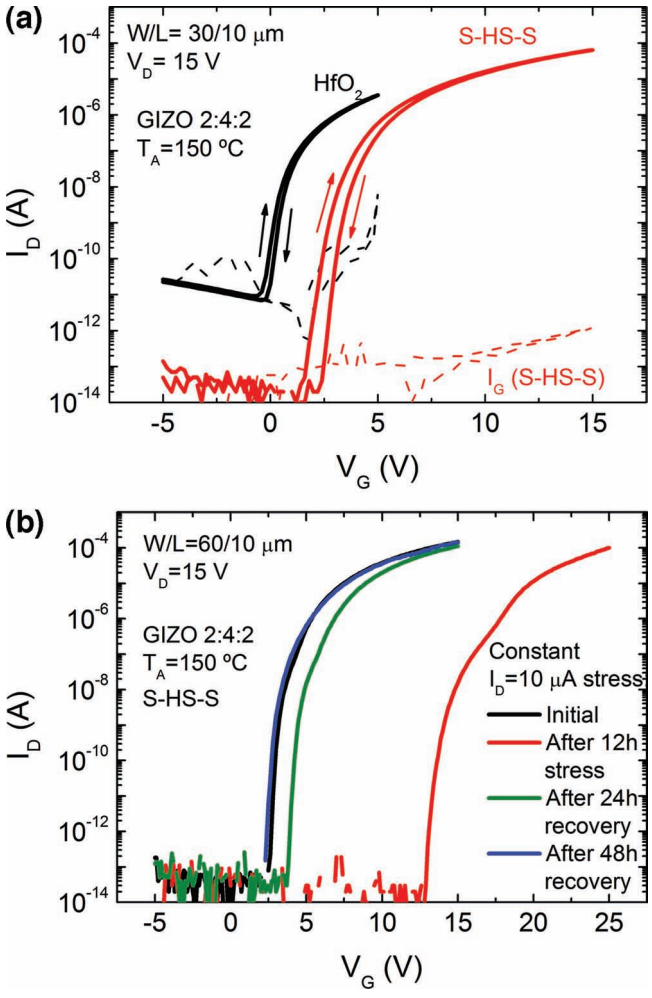


Figure 20. Electrical properties obtained for GIZO TFTs with Hf-based dielectrics: a) transfer characteristics for HfO_2 and S-HS-S devices; b) transfer characteristics evolution for S-HS-S TFTs during constant I_D stress measurements. Devices annealed at 150 °C.

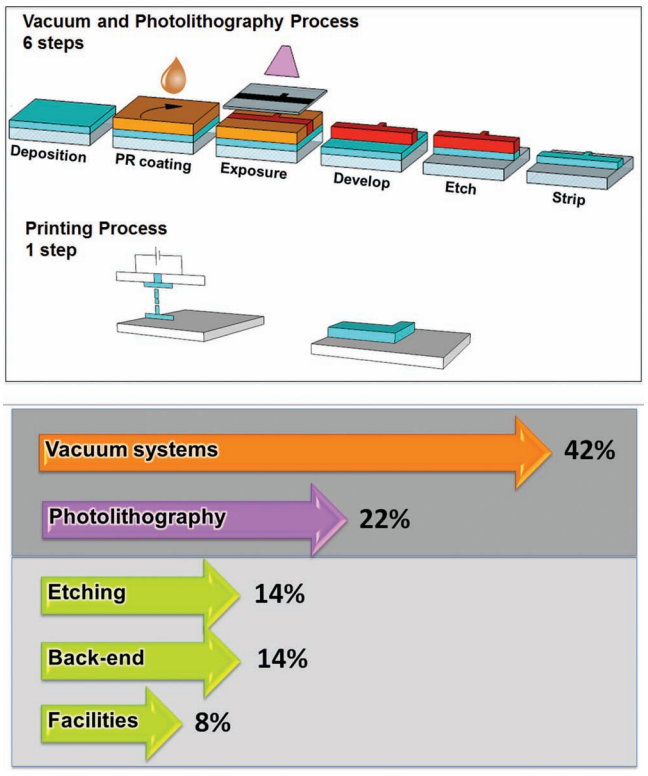


Figure 21. Comparison between printing process and conventional microelectronic technology as well as the costs (normalized) associated to each process.

Although many soluble organic semiconductors have been explored for this purpose, their functional performance generally falls short of expectation, in addition to other process issues. Low mobility, low current density, process-dependent performance variations and reliability issues are among the critical deficiencies with these materials, turning them inappropriate for applications like for example TFTs for active matrix backplanes for displays. On the other hand, inorganic semiconductors are the basis for almost all-high performance microelectronic devices. For example they can have intrinsic mobilities of ~1000 $cm^2 V^{-1} s^{-1}$, with lifetimes over 50 years and clock speeds beyond 1 GHz.

Ink-jet printing of inorganic materials for the formation of active devices is relatively new compared to the research done with respect to organic materials. To date, only a handful of inorganic materials have been ink-jet printed, primarily because of the difficulty in preparing ink-jet-printable precursors. Printing of functional inorganic materials is a challenging task with respect to processability and materials performance, especially for TFTs. There are many advantages to employing ink jet printing for electronic circuits: it is a digital process, no masks or screens are necessary; it is an additive process, materials are applied only where desired and it is a non-contact process, the print nozzles do not contact the substrate, preserving delicate surfaces.

Figure 21 compares the cost reduction between ink-jet and conventional microelectronic technologies, where a reduction of 64% is achieved by using for example direct printing.

The first efforts to print an electronic device backs to 1967, when Sihvonen et al.[322] inspired by the recent work reported by Weimer, has demonstrated the possibility to make an insulated gate field effect transistor (he call them *Graphic Active Devices–GAD's*) with all the materials printed: semiconductor based on CdS:CdSe inks; dielectric based on silicate cements and electrodes based on a Hg:In paste-like. Although these preliminary results were not spectacular (see **Figure 22**), this work can be considered as a landmark in the printed electronics history.

Printed electronics is today an emerging disruptive technology which has made an impressive progress specially in the last 10 years, in particular for: (i) the field-effect mobility of solution-processed organic TFTs has increased to levels exceeding those of amorphous silicon TFTs (~1 $cm^2 V^{-1} s^{-1}$);[19,323,324] (ii) the performance of polymer LEDs is surpassing that of fluorescent tubes[325] and (iii) the efficiency of printed organic solar cells is reaching levels of 5–8%.[326]

Ink-jet of inorganic materials for making active devices was relatively rare compared to organic materials, mainly due to

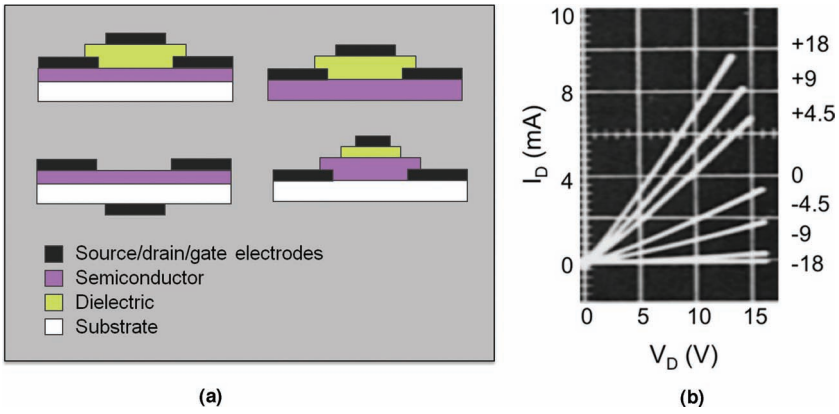


Figure 22. a) Examples of the tested insulated gate field effect devices used by Sihvonen et al. and b) Output characteristic of a device using an inorganic ink-dielectric layer (adapted from [322]).

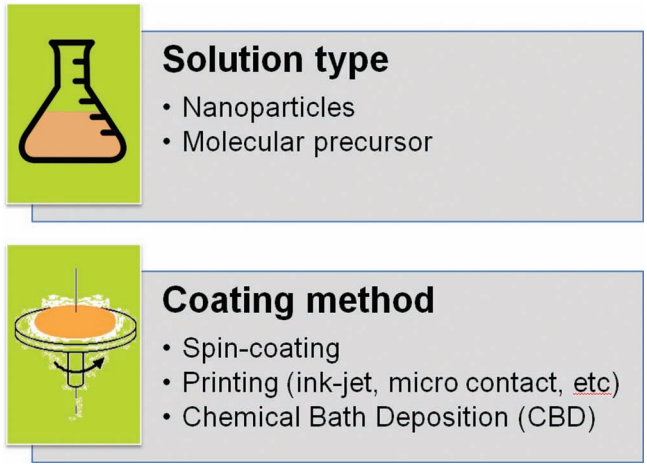


Figure 23. Solution type and coating methods used for solution-processed TFTs.

the difficulty in preparing ink-jet printable precursors.[327] Some efforts have been done in the last five years and basically two main routes have been followed: nanoparticles and molecular precursor approach. Concerning the coating method for a solution process the most used are: spin-coating; printing (ink-jet, micro contact, among others) and chemical bath deposition (see **Figure 23**).

Concerning the nanoparticle approach, usually the devices present some instability due to the large surface area of the nanoparticles. In opposition, the molecular precursors approach has the advantage of mixing different metal precursors in the same solution.

Although the possibility to deposit inorganic semiconducting films directly from a solution to achieve high levels of device performance was already reported in 2001 by Ohya et al.,[328] it is still challenging to obtain high mobility semiconductor layers at low temperatures. In their work the TFT mobility was 0.2 cm^2 V^{-1} s^{-1} and the on/off ratio was 10^7, but for a very high T_A, in the order of 900 °C. More recently, Adamapoulos et al.[329–331] succeed to increase the channel mobility of Li-doped ZnO TFTs processed at a temperature of 400 °C for values higher than 85 cm^2 V^{-1} s^{-1} using ambient spray pyrolysis and blends of precursor solutions based on zinc and lithium acetates (**Figure 24**). They use a bottom gate configuration and a high/κ dielectric based on ZrO_2 oxide layer also deposited by spray pyrolysis. Despite the fact that the semiconductor channel layer is not patterned, which in some cases over estimates the channel mobility,[332,333] these results evidence the potentialities of a very simple and low cost technology for device and circuit applications, whose main bottleneck is still the process temperature that limits the type of substrates that can be used. In 2007 Chang et al.[334] and Lee et al.[327] reported ZTO and IZO by spin coating respectively, at temperatures of 600 °C.

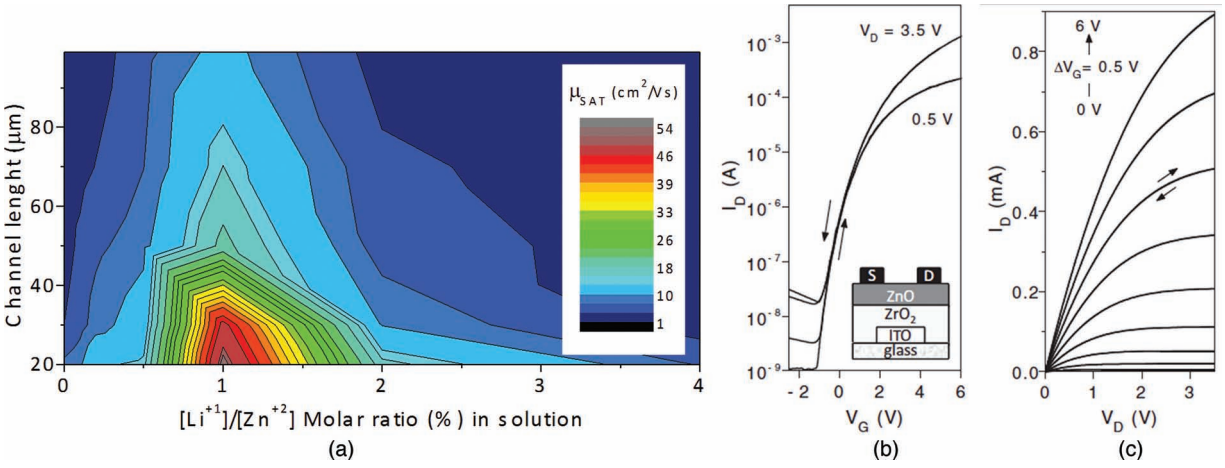


Figure 24. a) Contour plot of the field-effect electron mobility as a function of channel length (L) and the [Li+1]/[Zn+2] molar mass ratio;[330] b) Transfer characteristic (linear V_D = 0.2 V and saturation V_D = 3.5 V) and c) Output characteristics of bottom-gate, top-contact TFTs with channel width W = 500 μm and channel length L = 20 μm, fabricated with Li-doped ZnO films on a 126 nF cm^{-2} ZrO_2 dielectric (adapted from [331]). The inset shows the TFT architecture used.

Table 2a. Previous work on solution-processed ZnO oxide semiconductors.

Material	Process	Temp [°C]	Mobility [$cm^2 V^{-1} s^{-1}$]	On/off	Reference	Year
ZnO	Chemical bath	900	-	-	[328]	2001
ZnO	Spin coating	700	0.2	10^7	[11]	2003
ZnO NR	Spin coating	230	0.6	10^5	[341]	2005
ZnO NR	Spin coating	230	1.4	10^5-10^6	[342]	2006
ZnO	Chemical bath	100	0.25	10^5	[343]	2006
ZnO	Spin coating	500	5.25	10^5	[344]	2007
ZnO	Chem. Bath Dep.	700	3.5	10^5	[345]	2007
ZnO NR	Spin coating	270	1.2	10^6	[346]	2007
ZnO NW	Ink-jet	250	2-4	10^4	[347]	2007
ZnO NW	-	-	1175	10^7	[348]	2007
ZnO	Spin coating	70	0.56	10^4	[349]	2007
ZnO	Spin coating	400	1.63	10^6	[74]	2008
ZnO	Ink.jet and Spin coating	500, 300	6.1-IJ, 3.1SC	10^6	[350]	2008
ZnO NP	DC, SC	150	1.02×10^{-3}	-	[351]	2008
ZnO NP	Spin coating	150	8.4×10^{-3}	10^4	[74]	2008
ZnO-Zr	Spin coating	300	4.2×10^{-3}	-	[352]	2008
ZnO	Spray	400	15	10^6	[329]	2009
ZnO	Spin coating	500	5.26	-	[353]	2009
ZnO	Spin coating	200	1.1	10^3	[354]	2009
Li-ZnO	Spin coating	550	3.07	10^7	[355]	2009
ZnO NP	Spin coating	200	1.2×10^{-5}	10^3	[356]	2009
Li-ZnO	Spray	400	54	10^7	[330]	2010
ZnO	Spin coating	200	0.39	10^6	[357]	2010
ZnO	Spin coating	500	1.29	10^7	[358]	2010
ZnO	Spin coating	90	7.53	10^4	[359]	2010
ZnO QD	Spin coating	600	0.28	10^5	[360]	2010
ZnO NP	Spin coating	500	0.1	10^5	[361]	2010
Li-ZnO	Spin coating	400	0.31	10^3	[362]	2011
ZnO	Spray pyrolysis	370	24	-	[363]	2011
ZnO NR	-	450	8.5	10^4	[364]	2011
ZnO	Spray pyrolysis	400	85	10^6	[331]	2011

NP–Nanoparticles; NW–Nanowires; NR–Nanorods; QD–Quantum dots

Table 2b. Previous work on solution-processed ZTO, IZO, IZTO, AIO, IMO oxide semiconductors

Material	process	Temp [°C]	Mobility [$cm^2 V^{-1} s^{-1}$]	On/off	Reference	Year
ZTO	Spin coating	600	16	10^5	[334]	2007
SnO_x	Ink-jet	500	3.62	10^3	[365]	2007
IZO	Spin coating	600	16	10^4	[327]	2007
ZTO	Spin coating	500	1.1	10^6	[366]	2008
In_2O_3	Spin coating	400	43.7	10^6	[367]	2008
IZO	Spin coating	500	7.3	10^7	[368]	2008
ZTO	Spin coating	500	5	10^8	[369]	2009

They obtained mobilities of 16 $cm^2 V^{-1} s^{-1}$ using a bottom gate configuration and a 100 nm thick thermally grown SiO_2 dielectric on top of a silicon substrate.

More recently and due to the superior electrical properties of GIZO TFTs, in 2009 the first reports on solution-based GIZO TFTs start to appear (see **Table 2**c and **Figure 25**). From these results we would like to highlight the work of Yang et al.[335,336] where they report NP-GIZO TFTs using the hydrothermal method (180 °C @ 10 atm) to transform a solution type metal hydroxide into an oxide nanoparticle gel. After dispersing and spin coating the solution a post-bake at 95 °C was used. They got mobilities of 7.65 $cm^2 V^{-1} s^{-1}$ and on/off ratios of 10^7. In the same year Nayak et al.[337] present high performance a-GIZO TFTs obtained by sol-gel spin coating technique. A μ_{FE} = 5.8 $cm^2 V^{-1} s^{-1}$ (μ_{sat} = 9.6 $cm^2 V^{-1} s^{-1}$) with an on/off ratio of 5×10^7 and subthreshold swing of 0.28 V dec^{-1} were obtained.

So far, these methodologies have focused on the use of metal acetates, nitrates and halides in coordinating solvents and generally they require elevated temperatures, usually higher than 400 °C to complete precursor decomposition and avoid undesirable contamination of the semiconductor, which is incompatible with the use of plastic substrates and in some cases due to the different thermal expansion coefficients cracking could occur. Taking this into account, Banger et al.[338] have recently discovered a novel precursor approach to obtain ternary and quaternary oxide semiconductors, that is based on the use of organic-inorganic metal alkoxide precursors able to produce dense amorphous films. This approach allowed demonstrating for the first time solution-processed films of InZnO and InGaZnO that have comparable electronic performance as sputtered films, i.e., mobilities ~10 $cm^2 V^{-1} s^{-1}$ and similar threshold voltage stability with process temperatures as low as 230 °C (see **Figure 26**). This so called "sol-gel on chip" method allows a controlled low-temperature processing from metal alkoxide precursors that, without mediated hydrolysis, decompose only at higher temperatures.

In 2011 Kim et al.[339] succeed to produce In_2O_3, ZTO and IZO TFTs by solution process at a temperature as low as 200 °C by using a clever and new self-energy generating combustion chemistry. The main advantage of this technique is the possibility to perform the chemical reactions at a much lower temperature since the precursor is optimized

Table 2b. Continued

Material	process	Temp [°C]	Mobility [$cm^2 V^{-1} s^{-1}$]	On/off	Reference	Year
ZTO	Spin coating	500	14.1	10^8	[370]	2009
ZTO	Ink-jet	500	0.6	10^6	[369]	2009
IZTO	Ink-jet	600	30	10^6	[371]	2009
ZTO	Ink-jet	600	1.02	10^7	[372]	2009
AIO	Spin coating	350	19.6	-	[373]	2009
IZTO	Ink-jet	600	30	10^6	[374]	2009
ZTO-Zr	Spin coating	500	4.02	10^6	[375]	2010
ZTO	Spin coating	500	27.3	10^7	[376]	2010
ZTO	Ink-jet	500	4.98	10^9	[377]	2010
IZO	Spin coating	450	6.57	10^9	[378]	2010
Mg-IZO	Spin coating	450	2.7	10^8	[360]	2010
Al-ITO	Spin coating	500	13.3	10^7	[379]	2010
IZTO	Spin coating	400	90	10^5	[380]	2010
Sc-IZO	Spin coating	500	2.06	10^7	[381]	2010
Hf-IZO	Spin coating	500	1.94	10^6	[382]	2010
ZTO	Ink-jet	300	1.8	10^7	[383]	2011
ZTO	Spin coating	500	6.77	10^8	[384]	2011
IZO	Spin coating	230	~10	10^8	[338]	2011
AIO	Spin coating	250	2.37	10^6	[385]	2011
IGO	Spin coating	400	0.87	10^3	[386]	2011
IZTO	Spin coating	600	4.36	10^5	[387]	2011
ZTO	Spin coating	500	2.5	10^8	[388]	2011
Zr-ZTO	Spin coating	500	4.02	10^6	[389]	2011
ZTO	Spin coating	500	0.76	10^6	[390]	2011
ZTO	Spin coating	250	1.76	10^7	[339]	2011

Table 2c. Previous work on solution-processed GIZO oxide semiconductors. SWNT– Single wall nanotube

Material	Process	Temp (°C)	Mobility	On/off	Reference	Year
GIZO	Spin coating	400	2	10^5	[391]	2009
GIZO	Spin coating	400	1.25	10^6	[289]	2009
GIZO	Spin coating	400	0.05	10^4	[392]	2009
GIZO	Dip Coating	500	0.1-0.4	10^6	[393]	2009
GIZO	Spin coating	450	0.96	10^6	[394]	2009
GIZO	Ink-jet	450	0.03	10^4	[395]	2009
GIZO	Spin coating	95-hydrothermal	7.65	10^7	[336]	2010
GIZO	Spin coating	95-hydrothermal	2.3	10^6	[335]	2010
GIZO	Spin coating	400	0.85	10^6	[396]	2010
GIZO	Spin coating	400	5.8	10^7	[397]	2010
GIZO	gravure printed	550	0.81	10^6	[379]	2010
GIZO	Spin coating	600	1.3	10^4	[358]	2010
GIZO	Spin coating	500	0.5-2	10^7	[398]	2010
GIZO	Spin coating	600	6.4	10^7	[399]	2011
GIZO	Ink-jet	500	1.4	10^7	[400]	2011
GIZO	Spin coating	-	0.24	-	[401]	2011
GIZO SWNT	Spin coating	450	0.17	10^4	[402]	2011

for auto-combustion, a reaction that generates heat by its strong exothermic nature. In this way the oxide formation is done at low heating temperatures, which leads to the complete removal of organic constituents. The self-generated heat of synthesis provides a localized energy supply (similar to a laser annealing), eliminating the need for high, externally applied processing temperatures (see schematics in **Figure 27**). In this study they use a redox based combustion synthetic approach using as fuel acetylacetone or urea and nitrates as oxidizers. This group succeed to produce a flexible printed In_2O_3 TFT with a mobility of 6 $cm^2 V^{-1} s^{-1}$ for T_A = 200 °C on transparent polymer substrates (**Figure 28**).

Taking into account the increased interest associated to solution-processed TFTs, associate, **Figure 29** represents the evolution in the number of papers, where a visible increase is obtained especially for the last 2 years. Papers published until July 2011 are also presented.

Tables 2 summarize published work on solution-processed TFTs since 2001. We have decided not to include the values for V_{th} and subthreshold swing due to the lack of data.

As a general trend, it can be seen that multicomponent oxides such as ZTO and IGZO lead to the best overall performance, with some of the results obtained in TFTs already approaching the ones typically obtained when using physically deposited semiconductors. Even if the processing temperatures are in most of the cases relatively large (>400 °C), there is an increasing number of works where lower temperatures are being used, in some cases around 100 °C, potentiating the use of low cost and flexible substrates in association with printed electronics.

4.7. p-Type Metal Oxide Based TFTs: Emergent Devices

The enormous success of n-type oxide semiconductors and its application to TFTs has motivated the interest in p-type oxide based semiconductors also to be applied to TFTs. However, until now there is no report about p-type oxide TFTs with performance similar to that of n-type oxide TFTs. P-type oxide TFTs are mainly limited by the low hole mobilities since the mobility of valence band derived carriers is generally lower than that of conduction band derived carriers, as in the case of n-type conductivity. In fact comparing to what happened in organic TFTs we are facing exactly the same but in an opposite

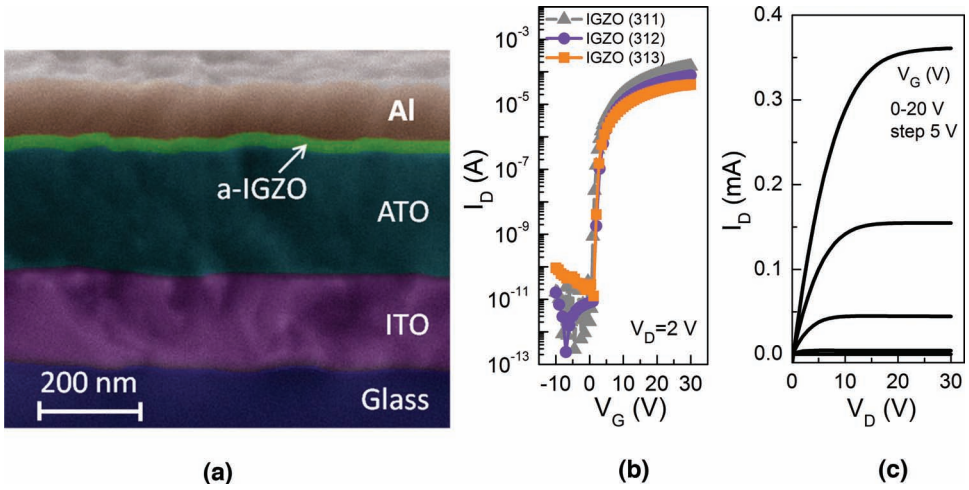


Figure 25. a) Cross sectional SEM image of GIZO (311) TFT; b) Transfer and c) Output characteristics of GIZO TFTs with different compositions (adapted from [337]).

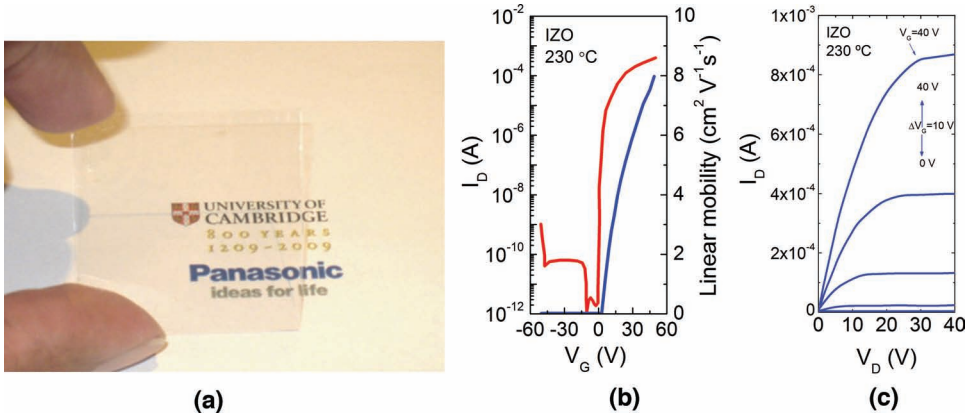


Figure 26. a) Photograph of a transparent, hydrolysed films; b) Transfer and c) Output characteristics of IZO TFTs produced under hydrolysed conditions (adapted from [338]).

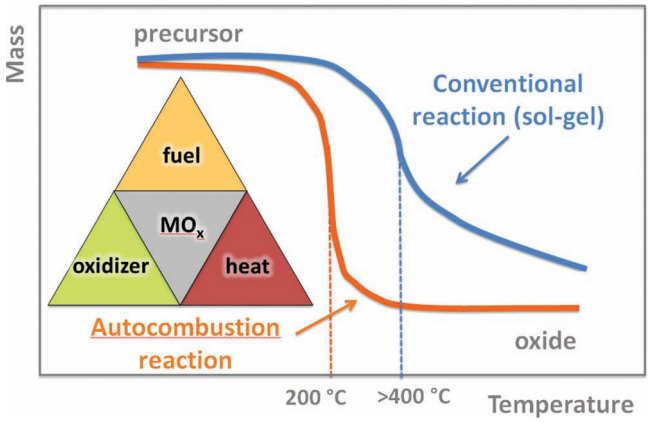


Figure 27. Schematic comparison of the decomposition profile of a combustion precursor and conventional sol-gel reaction (adapted from [340]).

way, since most of organic TFTs reported in the literature are p-type[403–406] while the oxide ones are n-type. Organic materials have been studied for more than 50 years and the significant improvements in the semiconducting properties associated to the discovery of electroluminescence in organic diode structures make these materials as excellent candidates for low-cost electronic and optoelectronic structures.[407,408] One of the main advantages of organic materials are the low temperature fabrication which allow lightweight flexible displays. Even though organic TFTs have been the topic of intense research for the past few decades, the overall performance parameters are still poor compared to oxide materials, namely the low mobilities (< 2 $cm^2 V^{-1} s^{-1}$)[409] poor stability and device-to-device variability as well as improved performance, processability, and environmental stability to oxygen and moisture. Moreover, the n-type organic semiconductors have much lower mobilities (10^{-2} to 10^{-1} $cm^2 V^{-1} s^{-1}$)[323,410–412] limiting their field of applications, such as in CMOS.

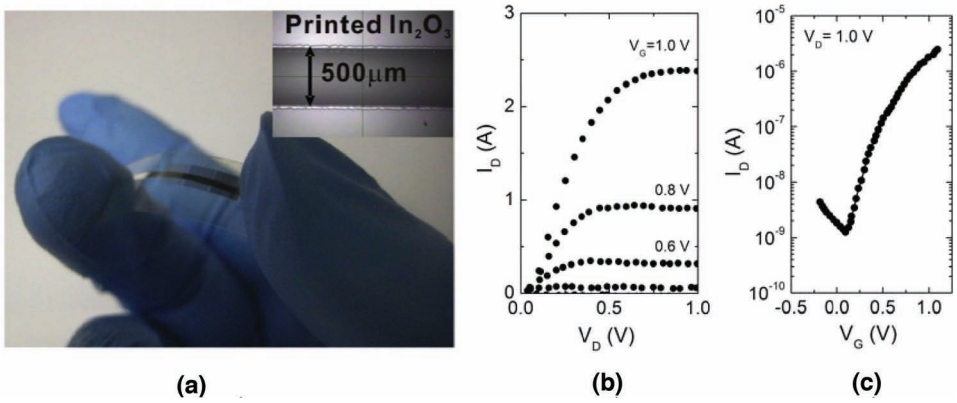


Figure 28. a) Optical photograph of a flexible combustion-processed In_2O_3 device on Acrylite (30 nm Al gate electrode/41 nm a-alumina dielectric, the inset shows an optical image of an ink-jet printed Al/41 nm a-alumina dielectric; b) output characteristics and c) transfer characteristics (adapted from [339]).

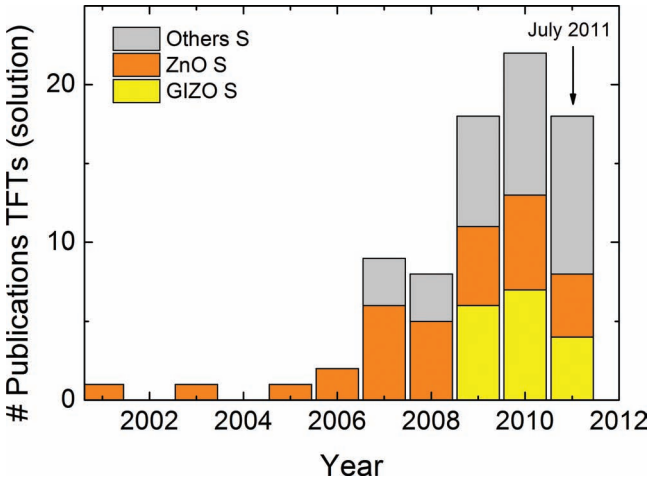


Figure 29. Number of solution-processed oxide TFTs related papers published per year. The data was taken from Tables 2a,b, and c.

Achieving high performance p-type oxide TFTs (that have an advantage over n-type TFTs since the TFT supplies hole current for the anode of the organic light emitting device [OLED] without affecting the drain current in the saturation mode) will definitely promote a new era for electronics in rigid and flexible substrates, away from silicon. Moreover, it will shape the electronics of tomorrow by allowing the production of complementary metal oxide semiconductors (CMOS), a key device to fuel the microelectronics revolution in the so-called technologies of information and communication, by allowing the use of highly compact circuits with low power consumption.

At present, almost all reported oxide TFTs are based on n-channel devices.[20,278] For p-type oxides, carrier conduction path (valence band) is mainly formed from the oxygen *p* asymmetric orbitals, which severely limit the carrier mobility. So, p-type oxides have very low carrier mobility compared to their n-type counterparts, which is the main obstacle in obtaining high performance p-channel oxide TFTs. Recently much attention has been given to Cu based semiconductors, of which the delafossite family $CuMO_2$ (M = Al, Ga, In, Y, Sc, La, etc.) is the most important. The simple binary oxides based on ZnO and NiO have also been studied as promising p-type semiconductors, but without relevant results until now.

In the following sections the discussion will be focused on the present available data on two emergent and promising p-type TFTs based on copper oxide and tin monoxide.

4.7.1. Copper Oxide

The first evidence of the semiconductor properties in a metal oxide was done on copper oxide, more precisely Cu_2O, cuprous oxide, in 1917 by Kennard et al.[413] (**Figure 30**a). Solid-state devices based on Cu_2O semiconductors are known for more than 90 years even before the era of germanium and silicon devices. Rectifier diodes based on this semiconductor were used industrially as early as 1926[414] (Figure 30b) and most of the theory of semiconductors was developed using the data on Cu_2O devices.[415–417]

Oxides of copper are known to show p-type conductivity and are attracting renewed interest as promising semiconductor materials for a wide range of optoelectronic devices. There are two common forms of copper oxide: cuprous oxide or cuprite (Cu_2O) and cupric oxide or tenorite (CuO). **Figure 31** shows a comparison between these two compounds in terms of optical properties and crystal structure.

Both the CuO (monoclinic) and Cu_2O (cubic) are p-type semiconductors with a band gap of 1.9–2.1 and 2.1–2.6 eV respectively[418] and in some experimental conditions Cu_2O shows mobilities exceeding 100 $cm^2 V^{-1} s^{-1}$.[419–422] Besides that, Cu_2O was regarded as one of the most promising materials for application in solar cells[28,423,424] due to its high-absorption coefficient in the visible region, non-toxicity, abundant availability, and low-cost production.[425] The potential for solar cell application have been recognized since 1920, nevertheless at that time and until the beginning of space explorations, the energy production from the sun by photovoltaic effect was just a curiosity.

The p-type character of Cu_2O is attributed to the presence of negatively charged copper vacancies (V_{Cu}), which introduce an acceptor level at about 0.3 eV above the valence band

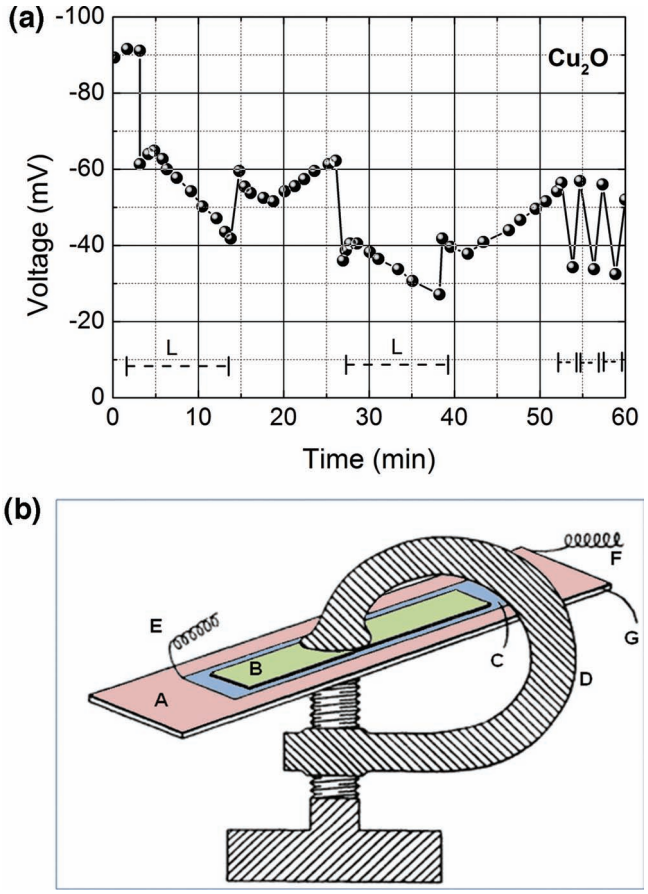


Figure 30. a) Evidence of the photo electromotive effect on Cu_2O. A series of readings of the potential at intervals of a minute, the dotted line marked L showing the periods of illumination. Apparently illumination produces, besides the sudden effect, a slow drift of potential followed by recovery in the dark but lagging by 2–3 minutes (adapted from[413]); b) Example of the first rectifier assembly. A is oxidized surface of copper strip; C is the piece of lead used for contact; B is mica insulation; and F is terminal connected to mother copper (adapted from [414]).

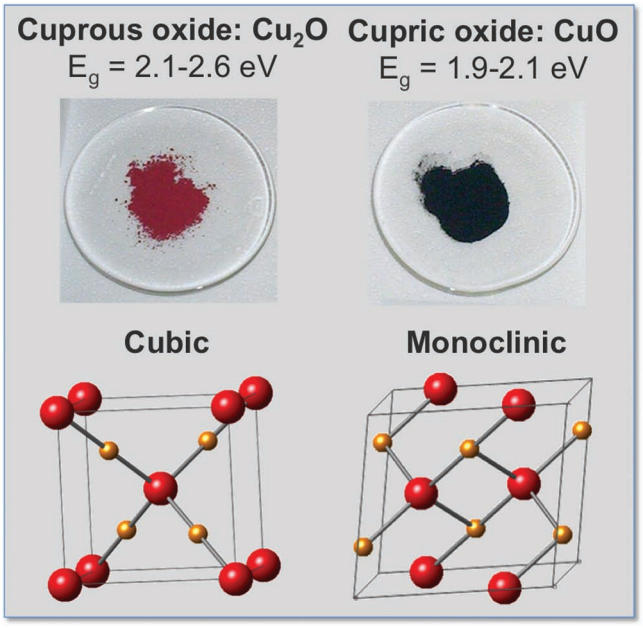


Figure 31. Copper (I) oxide or cuprous oxide is one of the principal oxides of copper. The compound can appear yellow or red, depending on the size of the particles. Cu_2O crystallizes in a cubic structure. Copper (II) oxide or cupric oxide belongs to the monoclinic crystal system. It is a black solid with an ionic structure.

(V_B).[426] It was also proposed by some authors a co-existence of both intrinsic, acceptor and donor levels with a ratio slightly larger than 1 and less than 10.[427,428] The nature of the donor levels is not completely clear being even controversial, where the simplest candidates are oxygen vacancies.[429] In contrast to the majority of metal oxides, in which the top of V_B is mainly formed from localized and anisotropic O 2p orbitals which leads to a low hole mobility due to hopping conduction, here the top of the V_B is composed of fully occupied hybridized orbitals (Cu 3d and O 2p) with Cu d sates dominating the top of the V_B.[430] **Figure 32**a illustrates the chemical bond between an oxide ion and a cation that has a closed-shell electronic configuration; Figure 32b shows a pictorial representation of the most important defects in Cu_2O and Figure 32c reveals the simple electronic model proposed by Brattain,[427] consisting of a compensated semiconductor with one acceptor level at 0.3 eV and a deep donor level at 0.9 eV from V_B.

High quality Cu_2O thin films have been grown by several methods, like sputtering,[432–435] pulsed laser deposition,[436–438] molecular beam epitaxy,[439] electrochemical deposition,[440–443] sol-gel,[444] plasma evaporation,[445] chemical vapour deposition[446] and thermal oxidation.[425,447,448] Among all these methods sputtering is a relatively cost effective process that can be used for large area deposition and thermal oxidation is the simplest, inexpensive and most conventional method to obtain copper oxide. It is well known that Cu oxidizes easily at low temperatures. This characteristic has impeded the application of Cu in integrated circuits. However, the high oxidation rate of Cu and high reduction rate of its oxides at low temperature can be exploited for some potential applications, as we will present in this paper.

Despite the high quality of CuO thin films with mobilities it has been difficult to produce TFTs with high channel mobilities. TFTs prepared from Cu_2O have shown very poor performance (field-effect mobilities and on/off current ratio were below 1 $cm^2\ V^{-1}\ s^{-1}$ and 10^2 respectively), mainly because of the difficulty of controlling the hole density in the channel layer.[431]

Generally in order to achieve high quality Cu_2O thin films the depositions involve high substrate temperatures, which is always higher than 500 °C. Recently it was shown by Li et al.[419] that it is possible to grow high quality Cu_2O thin films by reactive magnetron sputtering using a Cu target at temperatures in the order of 200 °C followed by a thermal treatment of 600 °C. In this work the authors found that with the introduction of a buffer layer the crystallinity increases associated to an increase in the grain size and under oxygen optimum growing conditions they achieved mobilities in the order of 256 $cm^2\ V^{-1}\ s^{-1}$ with a hole concentration of $10^{14}\ cm^{-3}$ as it is shown in **Figure 33**.

One of the first reports on p-type oxide based TFTs was proposed by the Wager's group using as channel layer a $CuZnO_x$

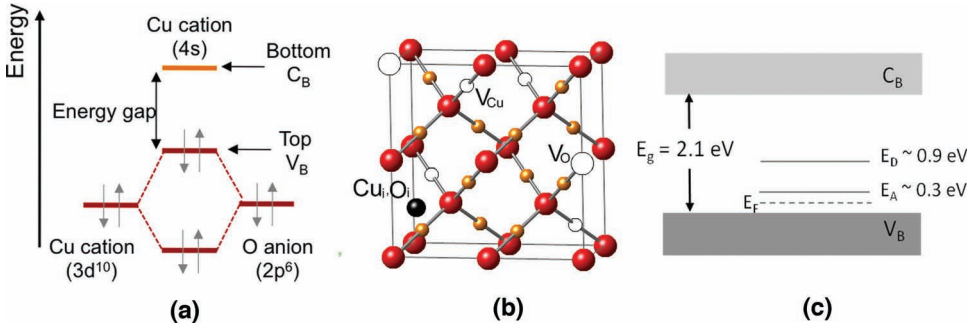


Figure 32. a) Chemical bond between an oxide ion and a cation that has a closed-shell electronic configuration; b) representation of the more important defects in Cu_2O; c) a simple electronic model proposed by Brattain, with a compensated semiconductor with one acceptor level at 0.3 eV and a deep donor level at 0.9 eV from V_B (adapted from [431]).

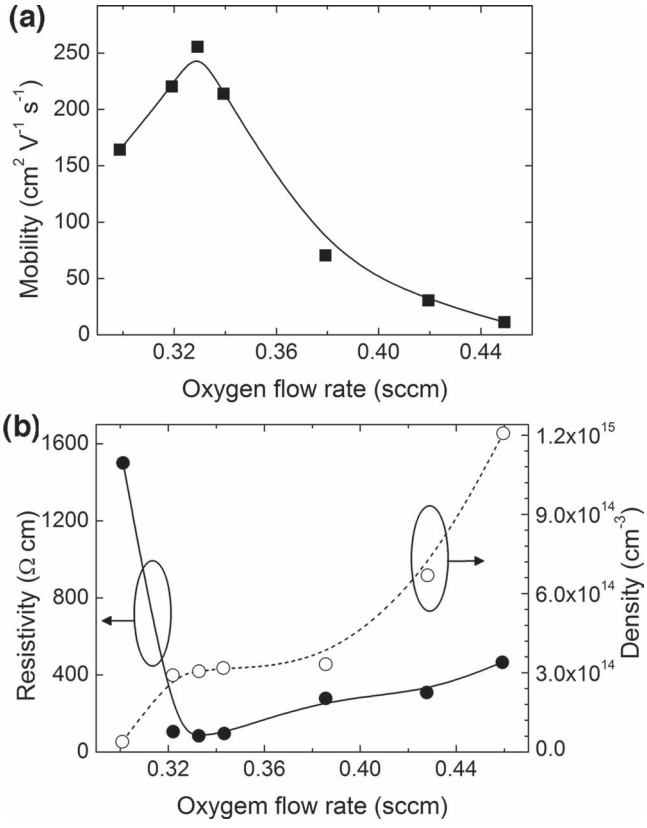


Figure 33. Mobility (a) and resistivity and hole density (b) of Cu_2O thin films with LTB-Cu_2O as a function of oxygen flow rates.[419]

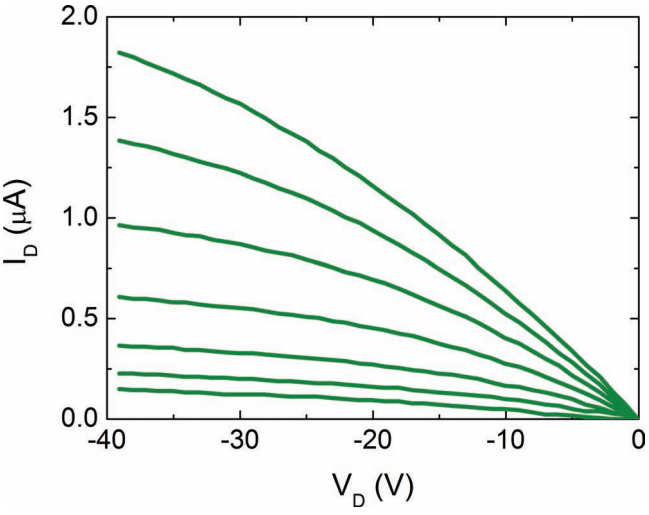


Figure 34. I_D–V_D curves for a p-channel TFT employing $CuZnO_x$ as the channel layer and a thermal SiO_2-silicon substrate bottom gate. The channel layer is subjected to a post-deposition furnace anneal in air at 800 °C in air. For this device, $V_{ON} \approx -60$ V, $\mu_{INC} \approx 0.01$ $cm^2 V^{-1} s^{-1}$, and W/L = 5 (adapted from [30]).

semiconductor[30] (**Figure 34**). This device shows poor performance with a very high ON voltage (≈–60 V) and a low channel mobility (≈0.01 $cm^2 V^{-1} s^{-1}$). Since V_{ON} is so large, the pinch-off condition was not achieved so that this device exhibits a "soft" saturation. Other detrimental features of this device include requiring an extremely high post-deposition annealing temperature of 800 °C which limits the use of low cost substrates and the fact that the channel layer is not completely transparent.

In the same year Matsuzaki et al.[420] reported TFT using single phase Cu_2O films grown by pulsed laser deposition at 700 °C on MgO substrates. Even though the hole mobility was very high (~90 $cm^2 V^{-1} s^{-1}$), the performance of the integrated TFTs were quite moderate (**Figure 35**). They have obtained mobilities of 0.26 $cm^2 V^{-1} s^{-1}$ and an on/off ratio lower than one order of magnitude. In order to investigate the origin of the obtained poor mobility, they subject the films to a post-deposition annealing under various oxygen partial pressures.[449] From optical measurements it was revealed that subgap states exist in all the films and their amounts were increased by post deposition annealing irrespective to the oxygen partial pressure used. These subgap states were observed even for the best film with an estimated defect density >10^{18} cm^{-3}. This value explains consistently the small field-effect mobility observed in these Cu_2O TFTs. The types of defects are mainly oxygen vacancies and the appearance of the CuO phase.

Two years later in 2010 Fortunato et al.[431] demonstrated the possibility to produce p-type transparent oxide semiconductors based on Cu_2O by reactive magnetron sputtering at

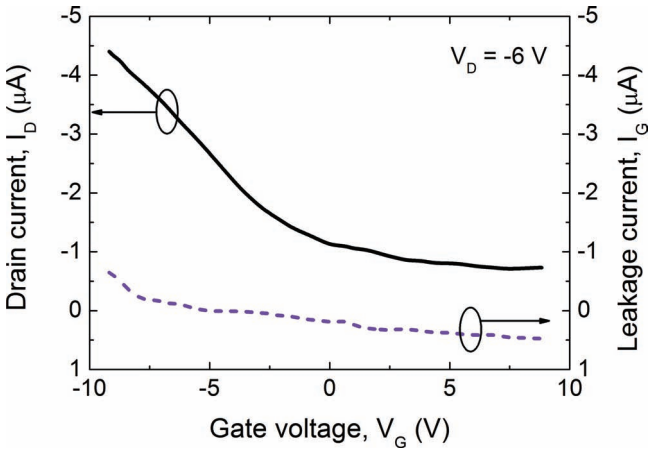


Figure 35. Transfer characteristic I_D–V_G of Cu_2O channel TFT at V_D = –6 V (adapted from [420]).

room temperature followed by a thermal treatment at 200 °C. The Cu_2O films are polycrystalline presenting a strong orientation along the (111) plane. After annealing in air at 200 °C for 10 hours, the Hall mobility was improved from 0.65 to 18.5 $cm^2\ V^{-1}\ s^{-1}$, which is associated with an increase of the grain size, from 8.30 to 15.72 nm. Concerning the optical properties, the p-type films present $E_{op} \approx 2.34$ eV and the films have an average transmittance around 85%, between 400 and 2000 nm for a thickness of 40 nm. Bottom gate p-type TFTs with Cu_2O channel layer present a $\mu_{FE} \approx 1.2 \times 10^{-3}\ cm^2\ V^{-1}\ s^{-1}$, an on/off modulation ratio of 2×10^2 and a V_T of –12.0 V as indicated in **Figure 36**.

Also in 2010 Sung et al.[450] have produced Cu_2O thin films deposited at room temperature using rf magnetron sputtering. For annealing temperatures higher than 200 °C a transformation to a CuO phase is observed. The obtained optical bandgaps of the Cu_2O and CuO were 2.44 and 1.41 eV, respectively. Bottom gate structured TFTs fabricated using CuO layers operated in a p-type enhancement mode with an on/off ratio of $\approx 10^4$ and field-effect mobility of 0.4 $cm^2V^{-1}s^{-1}$ (**Figure 37**).

The paper from Zou et al.[451] presented p-type TFTs based on CuO and Cu_2O with improved properties and in particular a mobility and on/off ratio of 4.3 $cm^2\ V^{-1}\ s^{-1}$ and 3×10^6 respectively, which re-opens the study on this semiconductor with almost 100 years. The films were grown on SiO_2/Si substrate by pulsed laser deposition under different substrate temperatures using a top-gate structure with a high-κ HfON as gate dielectric. The improved TFT mobility results from the decreased scattering of both the ionized defects and the grain boundary for Cu_2O channel films, which is also revealed by the low subthreshold, swing of 0.18 V dec^{-1} (**Figure 38**).

Table 3 summarizes the results achieved on p-type oxide TFTs as reported in the literature, concerning the technique, the deposition/annealed temperature, substrate/dielectric material, channel mobility and on/off ratio.

The obtained values for the channel mobility are much lower than that of the corresponding films, indicating that a high density of traps exists in the film channel or/and the channel/gate dielectric interface. Thus, trap states were still formed even in the high mobility films independent of the impurity phases.

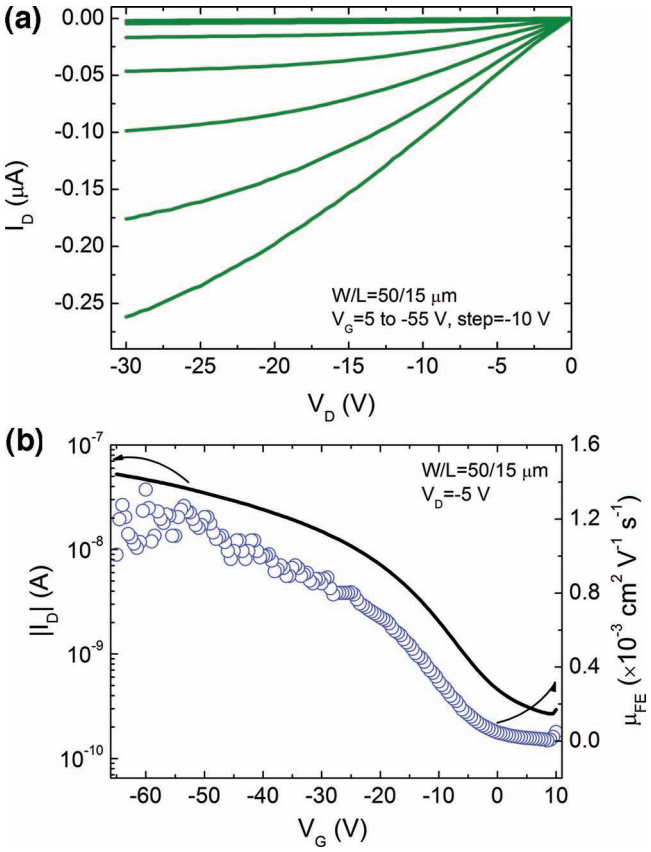


Figure 36. a) Output characteristics (I_D–V_D); b) Transfer characteristics ($|I_D|$–$V_G|$) at V_D = –5 V (left axis) and μ_{FE} as a function of V_G (right axis), for a typical Cu_2O TFT produced at room temperature and annealed in air at 200 °C. The inset shows the structure of the bottom gate TFT (adapted from [431]).

We consider that extra trap states would be formed by slight nonstoichiometry of Cu_2O or induced by the device fabrication process, e.g., by ion bombardment and/or plasma reduction during deposition of the other device layers.

Nevertheless, Cu_2O is a promising channel material for p-type oxide TFTs in the future. It is expected that further improvements on the electrical properties of the Cu_2O TFTs can be obtained if the device structure and processing conditions are optimized. The low temperature process combined with the good electrical performance of the devices at this early research stage opens new doors for the future optimization of p-type oxide-based devices and for their integration in CMOS structures allowing their use in flexible, low cost and transparent electronic circuits. As it was written by Wager in his book Transparent Electronics:[30] "The development of robust p-type semiconductors for use as channel materials in TFTs remains a considerable challenge, where considerable material development in needed before high performance devices can be realized."

Besides the physical techniques mentioned in the description above I would like to emphasize that, low cost p-type TFTs based on Cu_2O can be produced. Figueiredo et al. deposited thin films of Cu by e-beam evaporation at room temperature[425] followed by thermal oxidation at different temperatures in air. They

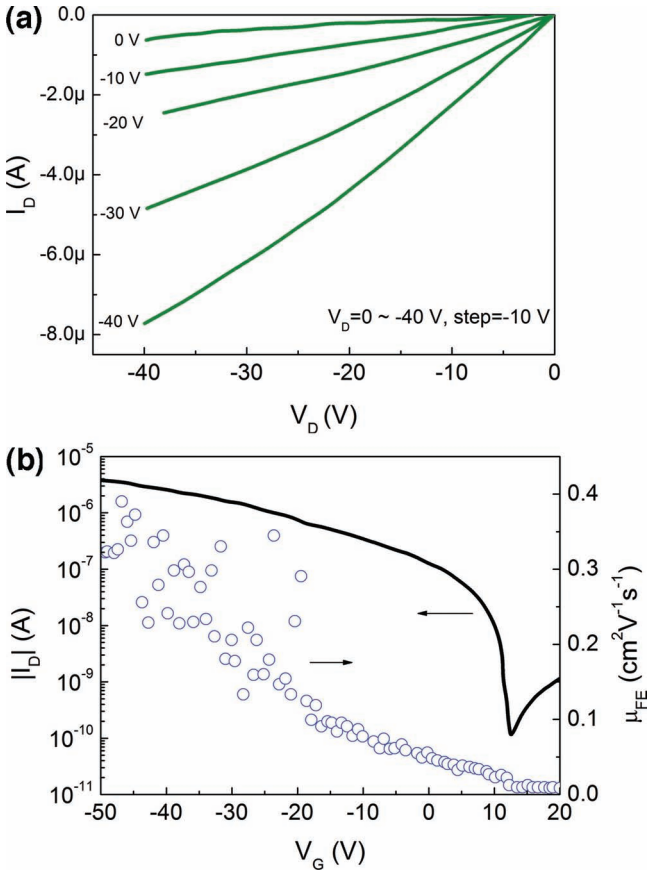


Figure 37. a) Drain current-drain voltage I_D-V_D characteristics of a thin-film transistor based on an active layer of the postannealed CuO at 300 °C. The gate voltage, V_G varied from 0 to 40 V in steps of 10 V and b) the source-to-drain current, I_D as a function of gate voltage, V_G at a fixed drain voltage of –10 V measured in air (adapted from [450]).

found that the cubic Cu phase of the as deposited films changes into single cubic Cu_2O phase for annealing temperatures below 300 °C and changes to monoclinic CuO phase at higher temperatures, which is in accordance with previous results.[454,455] The films with dominating Cu_2O phase show p-type conductivity. Based on these results a p-type TFT was produced and the preliminary results are presented in **Figure 39**.

The poor electrical properties obtained for these TFTs are related to the several micro-structural defects that occur during oxidation. The Cu ions migrate from Cu toward oxygen/Cu_2O interface with the formation of a porous layer.[456] This was confirmed by atomic force microscopy (AFM) for an oxidized film and a Cu_2O film grown by rf magnetron sputtering, where the surface roughness increases from 4.6 nm to 18.2 nm (**Figure 40**).

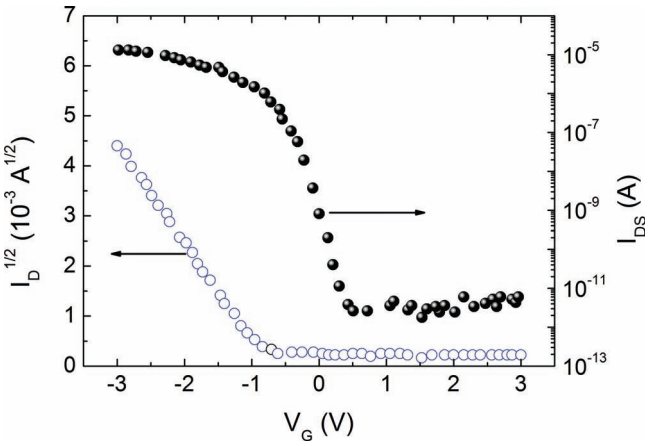


Figure 38. Transfer characteristics of p-channel Cu_2O TFTs with W/L = 500/20 µm. V_G was swept from –3 to 3 V at V_D = 3 V (adapted from [451]).

Another example using thermal oxidation of copper was presented by Han et al.[457] where a Cu wire is used for making a Cu_2O-Cu field effect transistor as it is indicated in **Figure 41**. The inner core Cu wire and outer shell Cu_2O film were used for the gate and channel respectively, and a Schottky barrier at Cu/Cu_2O was used for gate diode in the metal semiconductor field effect transistor. This particular cylindrical layout of the device can play the role of a fibber of the textile and the transistor therefore can serve as the fundamental building block for future e-textile.

4.7.2. Tin Monoxide

Tin oxides are known to be wide band gap oxide semiconductors and are present into two well-known forms: tin monoxide SnO and tin dioxide SnO_2. SnO_2 (and impurity doped SnO_2) is a typical functional material with multiple applications including transparent conducting oxides,[458,459] low emission windows coatings[460] and solid state gas sensing material.[461] In contrast, the physical properties of SnO have not been well explored. SnO_2 has a tetragonal structure and the unit cell contains two tin and four oxygen atoms. Each tin atom is at the centre of six oxygen atoms placed approximately at the corners of a regular octahedron, while each oxygen atom is surrounded by three tin atoms at the corners of an equilateral triangle. SnO

Table 3. State of the art concerning oxide p-type TFTs based on Cu oxide for the last 3 years.

Channel layer	Technique	T_{dep}/T_{post} [°C]	Substrate - Dielectric	μ [cm^2 V^{-1} s^{-1}]	On/off	Reference	Year
Cu_xO	PLD[+]	700	MgO–Al_2O_x	0.26	6	Matsuzaki et al.[420,449]	2008
	rf sputtering	RT/200	Si-SiO_2	0.4	10^4	Sung et al.[450]	2010
	PLD	500	Si/SiO_2 - HfON	4.3	3×10^6	Zou et al.[451]	2010
	rf sputtering	RT/200	Glass-ATO[*]	1.2×10^{-3}	2×10^2	Fortunato et al.[431,452]	2010
	PLD	500	Si/SiO_2–HfO_2	2.7	1.5×10^6	Zou et al.[453]	2011

[+])PLD–Pulsed Laser Deposition; [*])ATO - superlattice of Al_2O_3 and TiO_2.

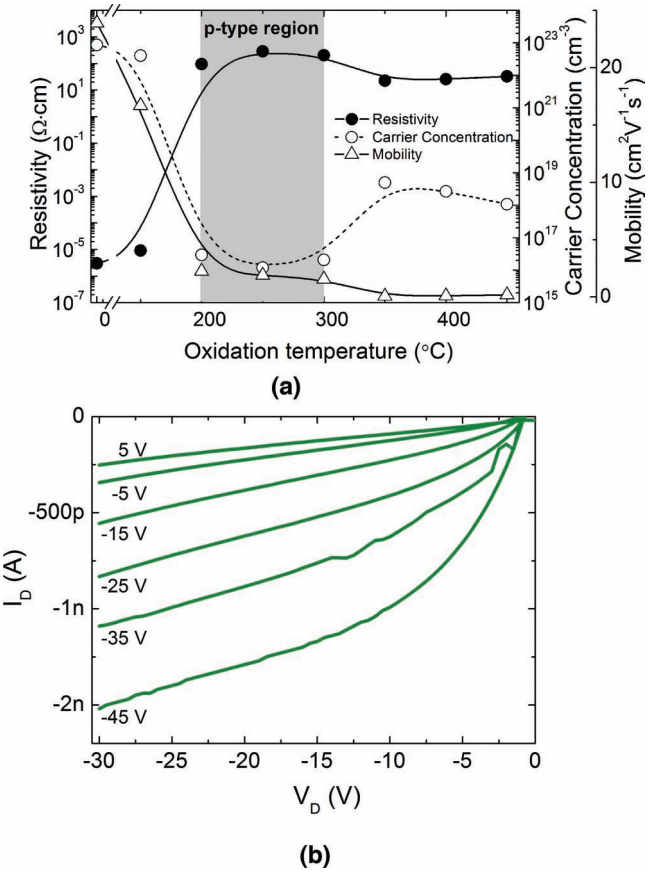


Figure 39. a) Dependence of the resistivity of Cu_xO films as a function of oxidation temperature; b) p-type TFT with Cu_2O channel layer oxidized in air at 200 °C.

has a specific electronic structure associated with the presence of divalent tin, Sn(II), in a layered crystal structure. The unit cells of SnO_2 and SnO are shown in **Figure 42**.

SnO_2 is an intrinsic n-type semiconductor and the electrical conduction results from the existence of defects, which may act as donors or acceptors. These defects are generally due to oxygen vacancies or interstitial tin atoms and are responsible for making electrons available at the conduction band.

In the past decades, due to its technological applications SnO have been used in a variety of applications like: anode materials for lithium rechargeable batteries,[462,463] coatings,[464] catalysts for several acids[465] and precursor for the production of SnO_2.[466] Recently, SnO has been received a particular attention because of the difficulty in obtaining stable and high quality p-type semiconductors based on ZnO,[467] NiO[468,469] and Cu_2O.[470] It was demonstrated by Togo et al.[471] that the p-type conductivity of SnO mainly originates from Sn vacancies.

TFTs based on p-type SnO_x are expected to fulfill these requirements due to the particular nature of band structure. Contributions from Sn 5s states to valence band maxima (VBM) could offer appreciable hole mobility in this material, without using a high processes temperature. The comparison between the band structure of SnO_2 and SnO is presented in **Figure 43**. In the case of SnO the top of the valence band consist of hybridized orbital of O 2p and Sn 5s.

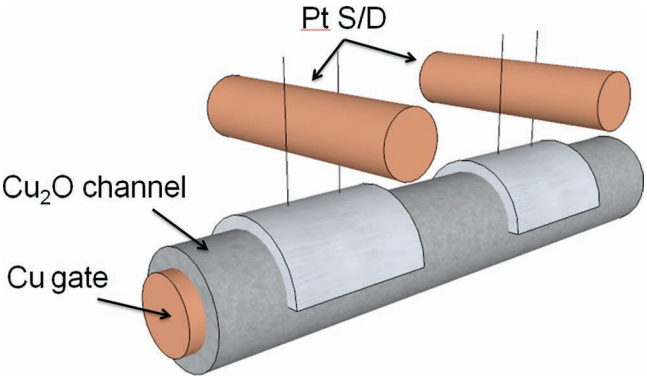


Figure 41. Schematic of Cu_2O transistor on Cu wire. Inner core Cu wire and outer shell Cu_2O film are used for the gate and channel, respectively. Source and drain pads are made by Pt by thermal evaporation, and the source and drain interconnection is made by cross-woven Cu wire, adapted from [457].

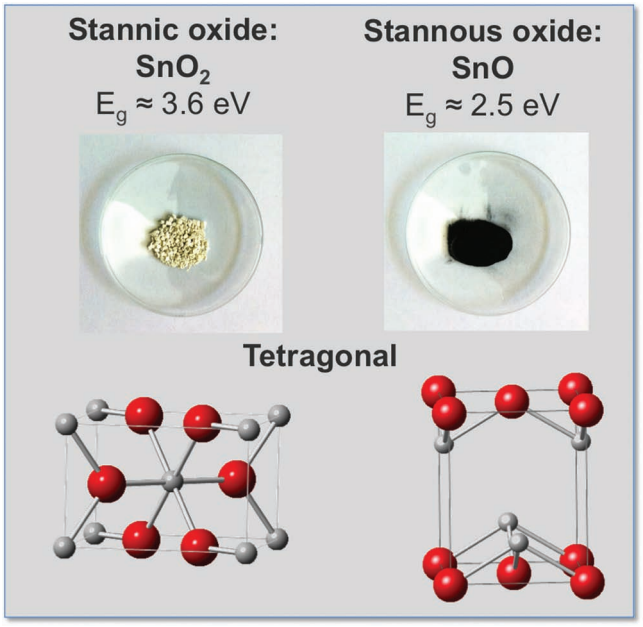


Figure 42. Unit cell of the crystal structure of SnO_2 and SnO.

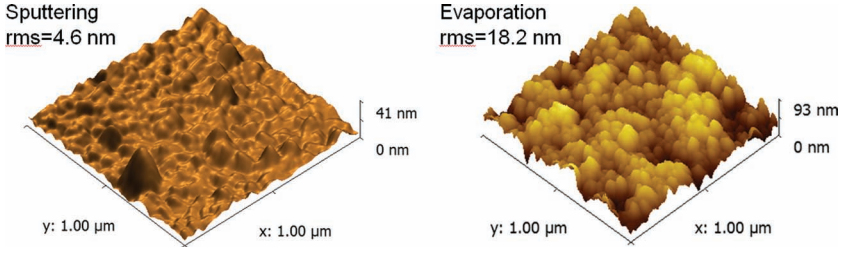


Figure 40. Surface roughness measured by AFM for a) a Cu_2O thin film grown by rf magnetron sputtering and b) a Cu_2O obtained by thermal oxidation of a Cu thin film.

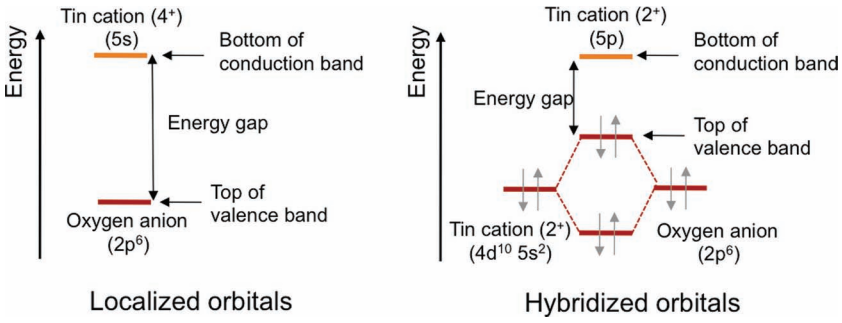


Figure 43. Comparison between the band structure of SnO_2 and SnO. In the case of SnO the top of the valence band consist of hybridized orbital of O 2p and Sn 5s.

The first p-type oxide based TFT was made in 2008 by Ogo et al.[472] using SnO as channel layer. The films were grown epitaxially on (001) yttria-stabilized zirconia at a substrate temperature of 575 °C by pulsed laser deposition. The films exhibit a Hall mobility of 2.4 $cm^2\ V^{-1}\ s^{-1}$ at room temperature. Top-gate TFTs, using the epitaxial SnO channels, exhibited field-effect mobilities of 1.3 $cm^2\ V^{-1}\ s^{-1}$, on/off current ratios of 10^2 and a threshold voltage of 4.8 V. In **Figure 44** we present the output and the transfer characteristics of this TFT. The TFTs operate in the depletion mode. The large off current associated to the depletion mode operation is attributed to the large hole density (>10^{17} cm^{-3}).

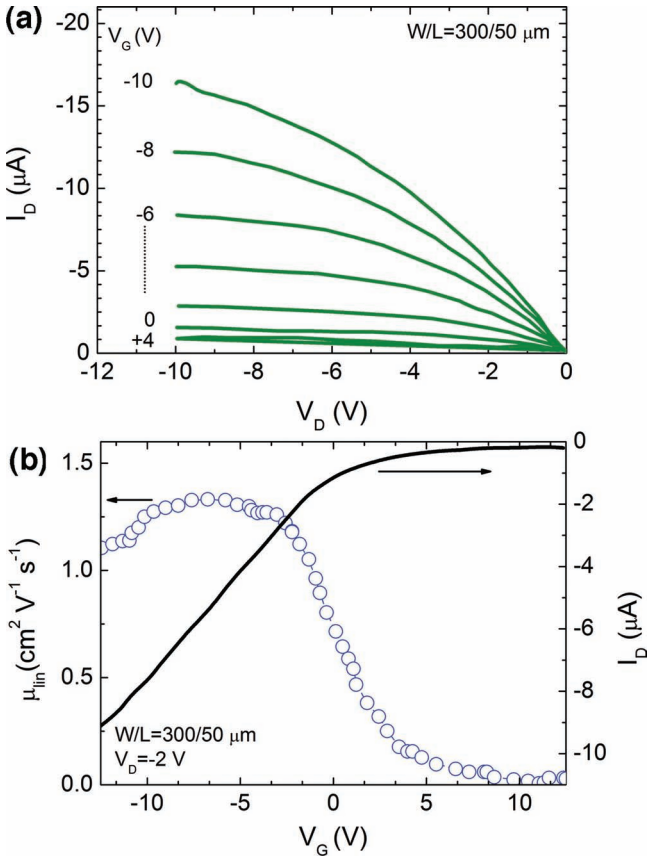


Figure 44. a) Output characteristics and b) field effect mobility in the linear region (μ_{in}) as a function of V_G (adapted from [472]).

In the same year two more papers were reported by Ou[473] et al. and Dhanajay et al.[474] SnO_2 was used for the channel semiconductor, deposited by reactive thermal evaporation at room temperature, followed by a post annealing in air at 100 °C. They used a bottom gate structure with SiO_2 thermally grown on Si wafer as dielectric layer and by tuning the post deposition temperature it is possible to control the electrical performance of the TFTs, specially the threshold voltage. The TFTs annealed at 100 °C present an on/off ratio of 10^3, field effect mobility of 0.011 $cm^2\ V^{-1}\ s^{-1}$, a threshold voltage of 30.4 V and subthreshold swing of 2 V dec^{-1} (**Figure 45**). The interface trap density at the semiconductor/dielectric interface obtained for this TFT was 8.1×10^{11} cm^{-2} which is very high, explaining the low value of channel mobility. The threshold voltage can be tuned using different post deposition temperature annealing and an inverter structure comprising two SnO_2 TFTs annealed at different temperatures was constructed. The obtained gain was calculated by differentiating the voltage transfer curve and it was found to be around 2.8. The same authors have also reported a hybrid complementary inverter composed with a p-SnO_2 and a n-In_2O_3 TFTs with an output gain of 11.[474]

In 2010 several reports on p-type SnO TFTs from Japan, Korea, Portugal and China have been published. Lee et al.[475] reported p-type TFTs by using a tin monoxide film deposited by vacuum thermal evaporation. The as deposited film showed as amorphous phase, and a polycrystalline tin monoxide was obtained by post annealing at 310 °C for 1 h in argon environment. They have fabricated bottom gate, bottom contact structure TFTs on heavily doped silicon wafers with a thermally grown silicon oxide layer. The TFTs performances are moderate, achieving an on/off ratio of 10^2 and a field effect mobility of 4×10^{-5} $cm^2\ V^{-1}\ s^{-1}$.

In the same year Liang et al.[476] reported p-type TFTs using amorphous SnO thin films deposited by electron beam

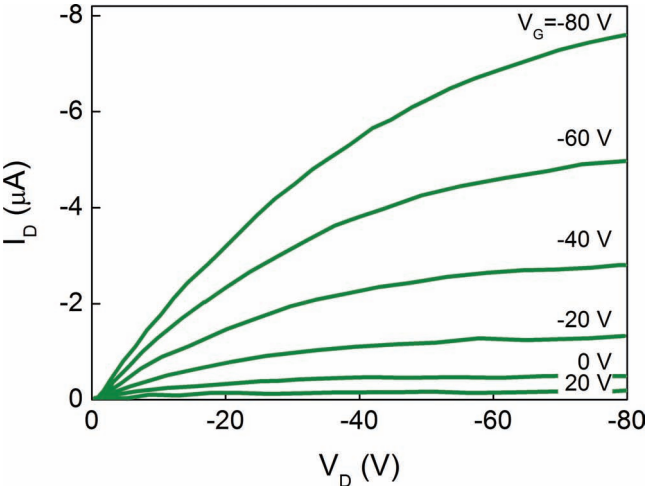


Figure 45. Drain current as a function of drain voltage at various gate voltages for the top-contact SnO_2 TFTs (adapted from[473]).

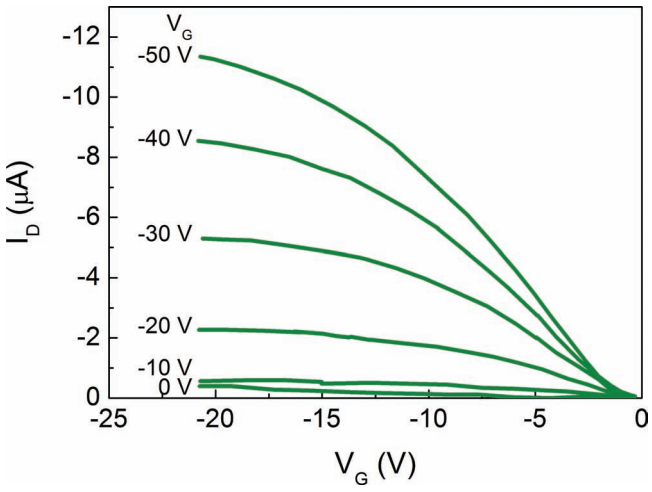


Figure 46. The characteristics of drain-source current (I_D) vs drain-source (V_D) for the TFT with the SnO channel annealed at 400 °C (adapted from [476]).

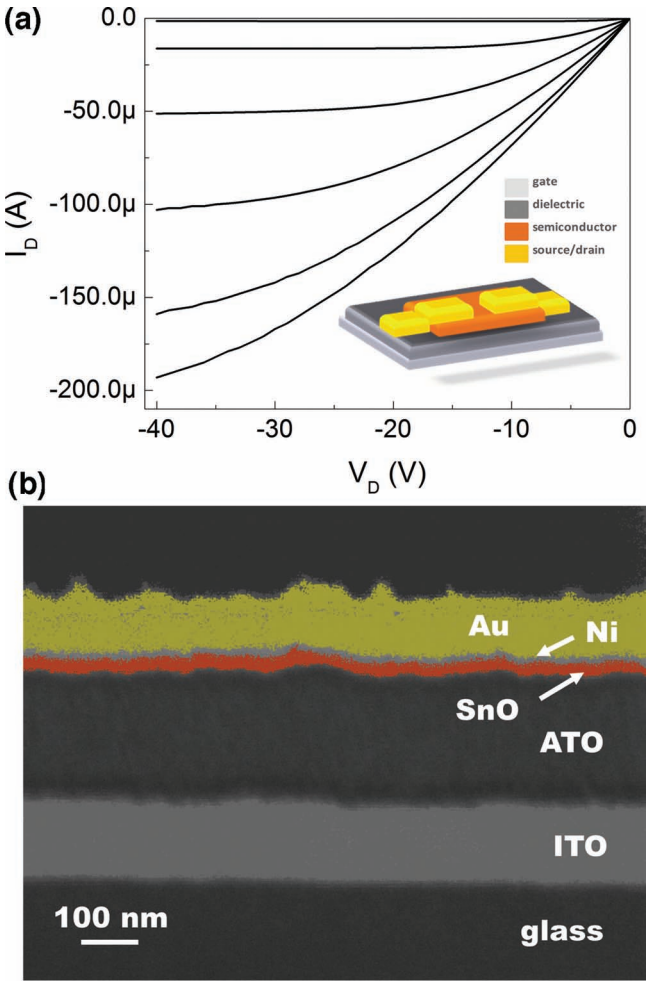


Figure 47. a) Typical output characteristic of SnO p-channel TFT (gate voltage is varied from 0 to –50 V in –10 V steps); b) TFT SEM cross-section where it is clearly shown all the constituent layers.

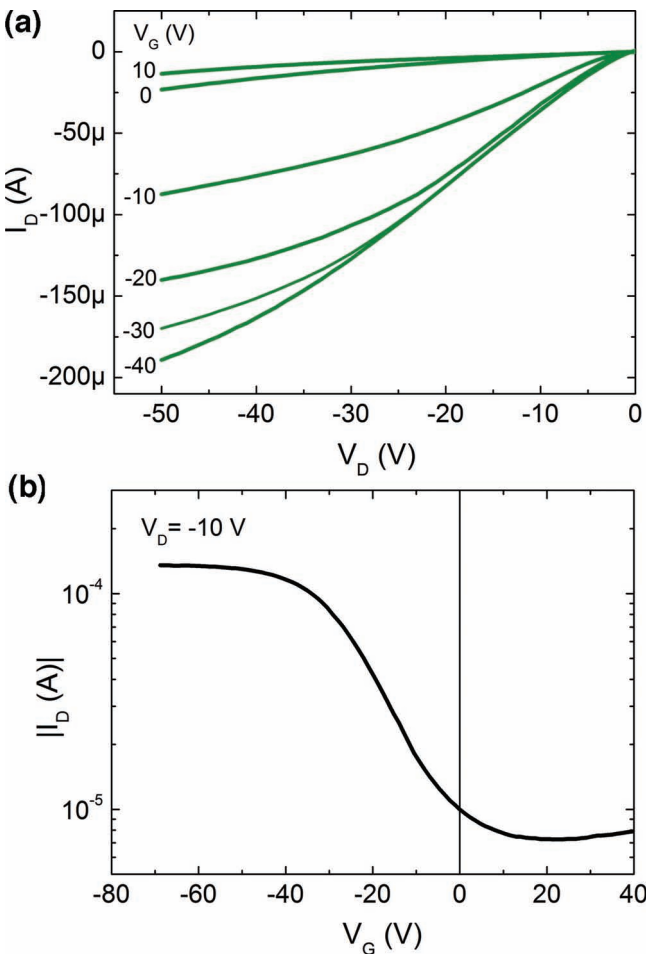


Figure 48. a) Output characteristics (I_D-V_D) and; b) Transfer characteristics ($|I_D$–$V_G|$), for a SnO_x p-type paper transistor produced at room temperature and annealed in air at 160 °C.

evaporation at room temperature followed by a rapid thermal annealing treatment in an argon atmosphere. Bottom gate TFTs using 100 nm SnO thick as channel layer have been deposited on top of SiO_2/Si substrates. The subthreshold swing, on/off ratio and field effect mobility are 11 V dec^{-1}, 2×10^2, –3.5 V and 0.87 cm^2 V^{-1} s^{-1} respectively (**Figure 46**).

Another p-type SnO TFT was reported in the same year by Yabuta et al.[477] Polycrystalline SnO thin films was used for the channel semiconductor by conventional rf sputtering with a subsequent annealing treatment. Bottom gate TFTs were fabricated using as dielectric layer a thin film of SiN_x formed by plasma enhanced chemical vapour deposition on n^+-Si. The TFTs exhibit an on/off ratio and field effect mobility of 10^2 and 0.24 cm^2 V^{-1} s^{-1}, respectively. The authors have also demonstrated in this report that oxidation of the SnO films decrease hole density and produce n-type SnO_2.

Fortunato et al. reported SnO_x TFTs deposited on glass substrate by rf magnetron sputtering at room temperature, followed by a rapid annealing at 200 °C. The SnO films present a polycrystalline structure composed with a mixture of tetragonal β–Sn and α–SnO phases, after annealing at 200 °C. These films exhibit

a hole carrier concentration in the range of ≈10^{16}–10^{18} cm^{-3}; electrical resistivity between 10^1–10^2 Ω cm; Hall mobility around 4.8 cm^2 V^{-1} s^{-1}; optical band gap of 2.8 eV and average transmittance ≈85% (400 to 2000 nm). Bottom-gate TFTs were fabricated using 30 nm thick α-SnO films as semiconductors, while the gate dielectric was a stacked multilayer of Al_2O_3 and TiO_2 (ATO) with 220 nm thick deposited on a glass coated with a 200 nm thick Indium Tin Oxide (ITO) film, acting as gate electrode. For the source-drain electrodes Ti/Au (8/50 nm thick) films were e-beam evaporated. The TFTs present a field-effect mobility above 1 cm^2 V^{-1} s^{-1} and an on/off modulation ratio of 10^3. More recently by controlling the SnO oxidation state it was possible to obtain TFTs with improved performance:[478] saturation mobility of 4.6 cm^2 V^{-1} s^{-1} and on/off ratio above 7×10^4, which are the highest values achieved so far in any p-channel oxide TFT (**Figure 47**).

In order to prove the feasibility of producing p-type oxide TFTs at room or/and low temperature we have produced a p-type paper-transistor using as dielectric layer a flexible cellulose sheet of conventional paper, based on a new concept "Paper Electronics - Paper-e" proposed by E. Fortunato et al. in 2008,[2,479,480] where the paper sheet works simultaneously as the substrate and the dielectric layer.

Figures 48a and b show the I_D–V_D and $|I_D$–$V_G|$ characteristics of a paper p-type SnO transistor after annealing in air at 160 °C.

The obtained electronic performances of the p-type paper-transistor do not differ significantly when the cellulose fibber is used as dielectric. The main difference is related to the on/off ratio, one order of magnitude lower, mainly related to the fact that cellulose fibbers have a typically open structure (macro-porosity), which limits the off current.

Figure 49a and b show a photograph and a schematic of the paper transistor, respectively. In Figures 49c and d we can see a scanning electron microscopy cross-section image of the gate electrode (IZO) deposited on one side of the cellulose paper. We can also observe the good step coverage of the IZO film along the cellulose fibbers.

In 2011 Nomura et al.[483] report the first ambipolar oxide-based TFT using an SnO channel semiconductor, and its application to a complementary-like inverter combining two ambipolar SnO TFTs. Saturation mobilities of 0.8 and 5×10^{-4} cm^2 V^{-1} s^{-1} are obtained for the p-channel and n-channel modes, respectively, and the inverter shows a maximum voltage gain of 2.5. The SnO films have been deposited by pulsed laser deposition at room temperature and bottom gate and top contact structures were fabricated on thermally oxidised SiO_2/n^+Si substrates. The devices were annealed at 250 °C in air. This result is the first demonstration of a complementary-like circuit using a single oxide semiconductor channel and provides an important step toward practical oxide electronics. More details in section 5.3.

Table 4 lists the p-type TFTs with SnO channel layer.

5. Emerging Applications

5.1. Displays with Oxide-Based Backplanes

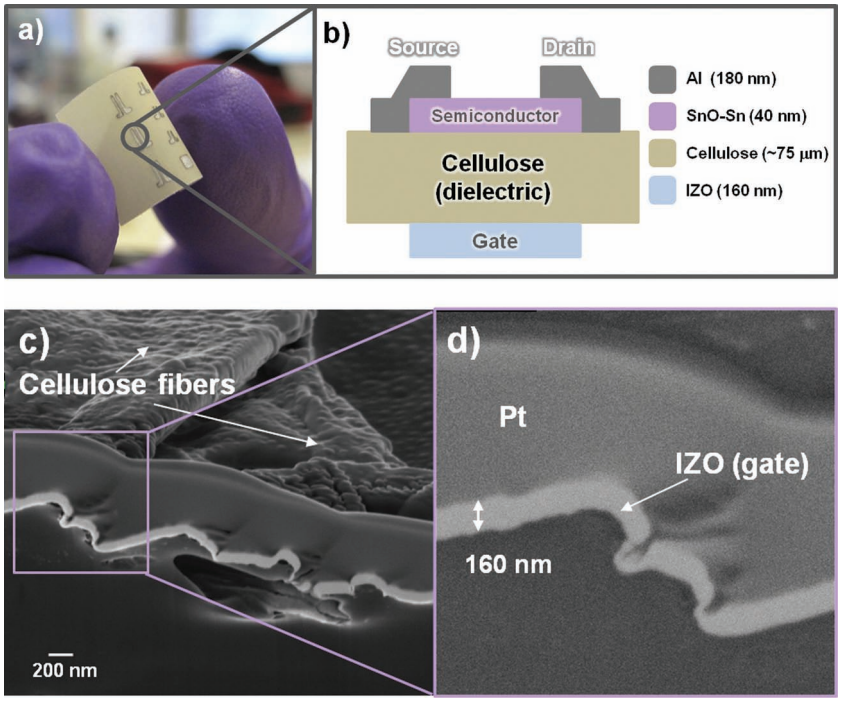


Figure 49. a) shows an optical photograph of a p-type paper transistor; b) architecture of the paper transistor; c) scanning electron microscopy cross section image of the gate electrode (IZO[481,482]) and d) with a higher magnification to see the detail of the good step coverage of the oxide semiconductor over the cellulose fibbers.

Given the close relation between TFTs and displays, it is not strange that the most significant application of oxide TFTs is on displays, mostly LCDs and OLEDs. From 2007, Soc. Information Display (SID) and International Meeting on Information Display (IMID) exhibitions have been the stage for the presentation of several prototypes employing oxide TFT technology.

At CENIMAT|I3N, oxides have been used both for passive matrix (PM) and active matrix (AM) backplanes (the integration of the PM and AM backplanes presented here with frontplane technologies was done at Centro Ricerche Fiat Italy and Hewlett Packard Ireland, respectively, under the framework of Multiflexioxides FP6 project). The PM backplane was produced using room temperature sputtered IZO,[481,484] patterned using conventional photolithographic processes, on 5 × 3 cm glass and polymeric substrates. Transparent alphanumeric displays with 7 segments, usable as head-up displays (HUDs) in automotive industry, were obtained by integration with chipLED frontplane technology (**Figure 50**).

AM backplanes for 2.8" LCDs were fabricated on glass, consisting of an array of 128 × 128 pixels, with each pixel having an

Table 4. State of the art concerning oxide p-type TFTs.

Channel layer	Technique	T_{dep}/T_{post} [°C]	Substrate-Dielectric	μ [$cm^2 V^{-1} s^{-1}$]	On/off	Reference	Year
SnO_x	PLD+	575/200	YSZ–Al_2O_x	1.3	~10^2	Ogo et al.[472]	2008
	Evaporation	RT/100	Si–SiO_2	1.1×10^{-2}	~10^3	Ou et al.[473]	2008
	Evaporation	RT/100	Si–SiO_2	4.7×10^{-3}	~10^2	Dhananjay et al.[474]	2008
	Evaporation	RT/310	Si–SiO_2	4.0×10^{-5}	~10^2	Lee et al.[475]	2010
	rf sputtering	RT/400	Si–SiN_x	0.24	~10^2	Yabuta et al.[477]	2010
	Evaporation	RT/400	Si–SiO_2	0.87	~10^2	Liang et al.[476]	2010
	rf sputtering	RT/200	Glass–ATO*	1.2	~10^3	Fortunato et al.[452]	2010
	rf sputtering	RT/200	Glass–ATO*	4.6	7×10^4	Fortunato et al.[478]	2011
	PLD+	RT/250	Si–SiO_2	0.75	~10^3	Nomura et al.[483]	2011

+)PLD–Pulsed Laser Deposition; *)ATO - superlattice of Al_2O_3 and TiO_2.

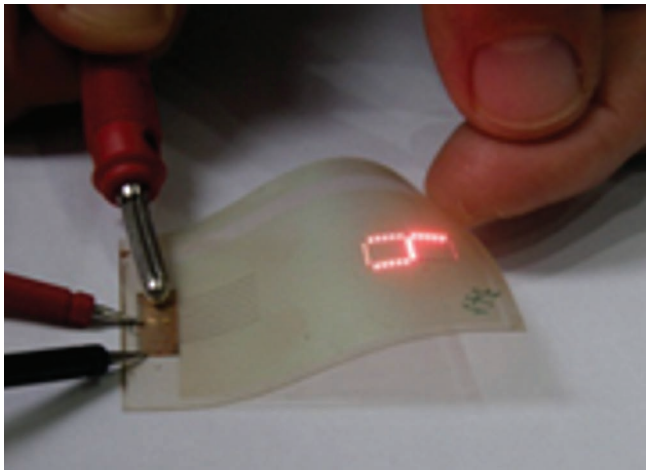


Figure 50. Transparent PM chipLED display using IZO electrodes.

approximate area of 350 × 350 μm (**Figure 51**a and b).[303] For demonstration purposes, the architecture was the simplest possible, with a single TFT per pixel. Backplane production consisted on a standard 5 mask process, using either Ti/Au or IZO source-drain and gate electrodes (for opaque and transparent AMs, respectively), GIZO channel layer, TSiO dielectric and SU-8 passivation. Finally, the final backplanes were annealed at 150 °C. The AM backplanes were then successfully integrated with reflective LCD frontplanes (Figure 51c). Still, evidences of some shorted gates were observed and attributed to the lack of reliability and reproducibility of the TSiO dielectric.

Several companies are currently working on oxide TFTs for demonstrating flexible and/or transparent displays. Some examples, all driven by GIZO TFTs, are the works from Samsung SDI, with a 4.1" 176 × 220 resolution full-colour OLED display, having a transmittance higher than 20%;[279,485] from LG Electronics Inc., with a 3.5" 176 × 220 resolution OLED display on a 0.1 mm thick stainless steel plate;[486] from Toppan Printing Inc., with 4" 320 × 240 resolution electrophoretic display on polyethylene naphthalate (PEN) plastic substrate (**Figure 52**a).[487] With atomic layer deposited ZnO TFTs, Park et al. also reported a 2.5" 220 × 176 resolution OLED transparent display on a glass substrate.[488]

But even when transparency of the overall display is not persuaded, oxide TFTs are of great interest. Their high mobility and large area uniformity can yield high-end displays, such as the 70" ultra-definition (UD) LCD 3DTV with a high scanning frequency (240 Hz) demonstrated by Samsung in 2010.

In most of the reported displays employing oxide TFTs, the channel layer is produced by sputtering. But despite the early stage of research on solution-processed oxide TFTs, LCD and OLED displays were already fabricated using this lower cost processing technology. In 2008, Chiang et al. reported sol-gel $Zn_{0.97}Zr_{0.03}O$ TFTs driving a 4.1" LCD display.[489] The first demonstration with OLEDs is attributed to Samsung Electronics, with a 2.2" monochromatic display with 128 × 160 resolution (Figure 52b), being the spin-coated IZO TFTs processed at a maximum temperature of 350 °C.[490] Other works followed, with increased panel sizes and resolution, such as the 4.1" LCD display with 320 × 240 resolution driven by spin-coated GIZO TFTs reported by Taiwan TFT LCD Association (TTLA)/Inpria Corp./Oregon State University.

The stage is now set for a variety of displays using oxide TFT technology, with small area flexible OLEDs and large area rigid high-end LCD and OLED displays being probably the main targets for commercial products in the near future. The numerous prototypes already shown by most of the greatest display companies is certainly an indication that products within the "transparent electronics" concept or, employing oxide semiconductors but not necessarily resulting in transparent displays, should not be far from entering in our daily life. In fact, as pointed out in the introduction, mass-production of the first transparent 22" LCD panels was already announced by Samsung in 2011. These displays exhibit a 1680 × 1050 resolution, a contrast ratio of 500:1 and a transparency of 15%. Instead of a backlight, ambient light is used, resulting in a 90% decrease in power consumption when compared with conventional LCDs.

5.2. Inverters and Ring Oscillators

For any semiconductor technology, the fabrication of inverters and ring oscillators (ROs) is a basic requirement for producing

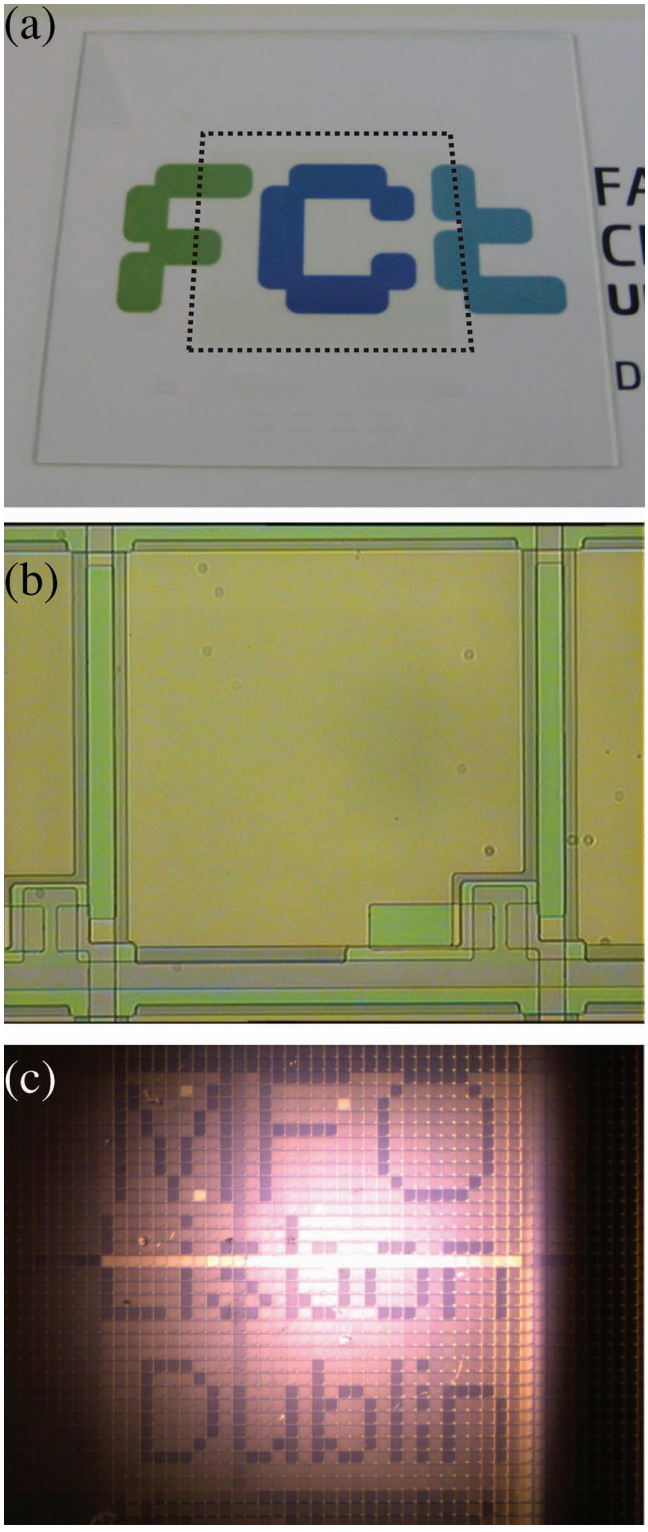


Figure 51. AM backplane with GIZO TFTs produced at CENIMAT for a LCD display: a) photograph of a transparent AM on glass; b) microscopy image of pixel area (350 × 350 μm); c) prototype after integration with LCD front plane.[303]

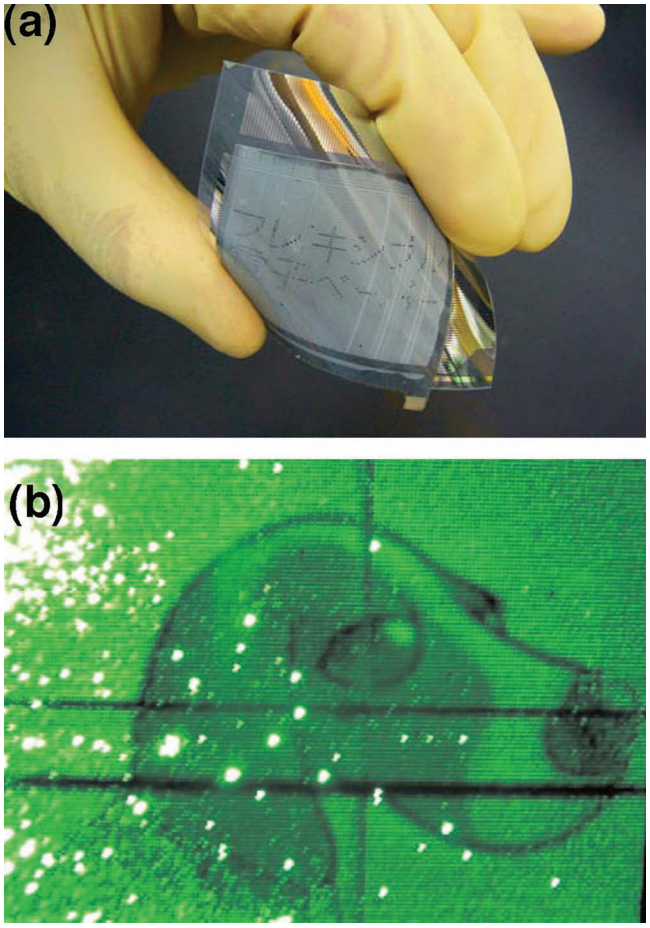


Figure 52. Prototypes of displays with oxide TFT backplanes: a) flexible electrophoretic display;[487] b) OLED display driven by solution-processed IZO TFTs.[490]

a complete range of logic circuits. A simple inverter is composed by two transistors (control and load). When the input voltage (V_{IN}) is low the control transistor is in the *off*-state and the load transistor pulls the output (V_{OUT}) to a "high" level. When V_{IN} is high, current flows through the control transistor, causing the output to be at a "low" level. A RO consists of any odd number of inverters connected in series. The evaluation of the performance of these simple circuits can provide a valuable tool to define the range of applications of a TFT technology. For instance, the propagation delay of a RO is a widely accepted benchmark regarding how fast a TFT can operate.[225]

To the authors' knowledge, the first transparent circuits with oxide semiconductors were reported in 2006 by Presley et al.[491] The authors reported sputtered IGO TFT based inverters and five-stage ROs on glass. **Figure 53**a shows the voltage transfer characteristic (VTC) of the inverters, which present a peak gain magnitude (dV_{OUT}/dV_{IN}) of ≈1.5. A maximum oscillation frequency of 9.5 kHz and a propagation delay of 11 μs/stage are achieved for the RO. These values are significantly affected by the large parasitic capacitance arising due to the large source/gate and drain/gate overlap, used here to facilitate device fabrication.

Finer design rules and improved TFT performance allowed Ofuji et al.[225] to report in 2007 five-stage ROs based on GIZO TFTs with considerably improved performance, such as an oscillation frequency of 410 kHz and a propagation delay of

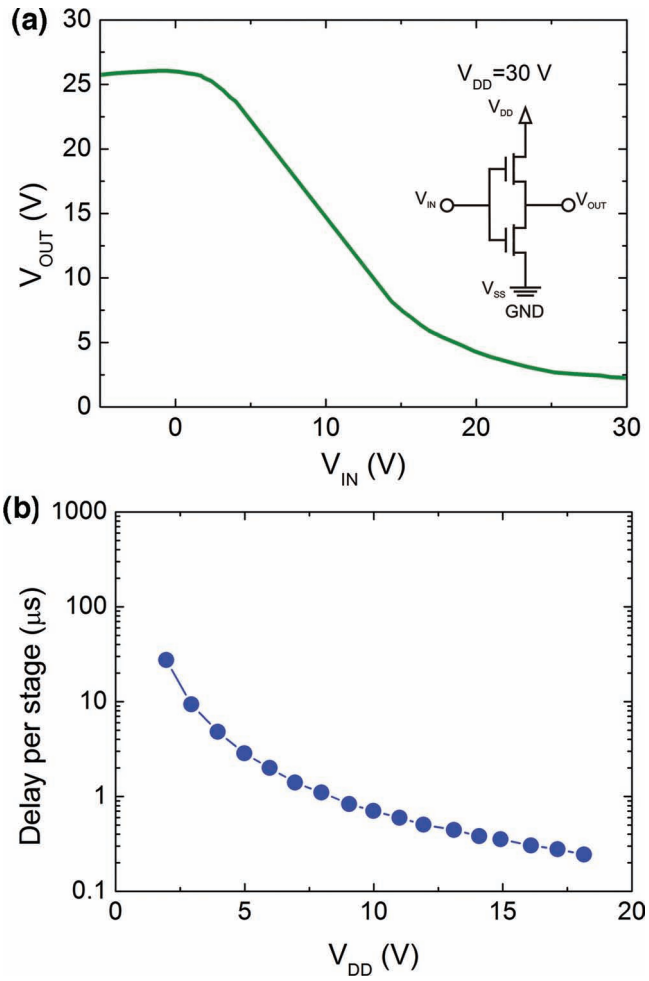


Figure 53. Electrical properties of initial oxide TFT based circuits: a) VTC for a transparent inverter using IGO TFTs (adapted from [491]); b) Propagation delay in a RO based on GIZO TFTs (adapted from [225]).

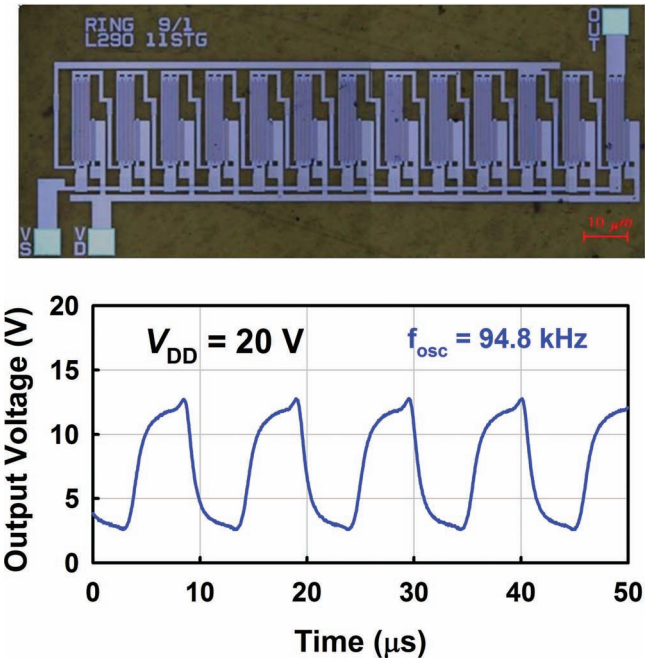


Figure 54. a) Optical image of an eleven-stage RO, and b) output characteristics of the fabricated ring oscillator on plastic substrates (adapted from [220]).

0.24 μs/stage (Figure 53b). The authors report that the propagation delay achieved in this work is half and almost one third of the ones achieved using a-Si:H and organic TFTs, respectively.

In 2008 the fastest oxide circuits on glass were reported by Sun et al.[492] ALD deposited ZnO TFTs processed at 200 °C were used to fabricate a seven-stage RO that operates at 2.3 MHz, corresponding to a propagation delay of only 31 ns/stage.

In 2011, eleven-stage ROs were also fabricated on flexible substrates by Mativenga et al.,[220] requiring maximum processing temperatures of 220 °C. These operate at a frequency of 94.8 kHz with a propagation delay of 0.48 μs/stage. The authors also reported a flexible two-clock shift register (gate driver) with AC operation. Based on gate bias stress measurements, an estimated lifetime of more than 10 years is announced for the gate driver, which is highly promising for flexible display applications (**Figure 54**).

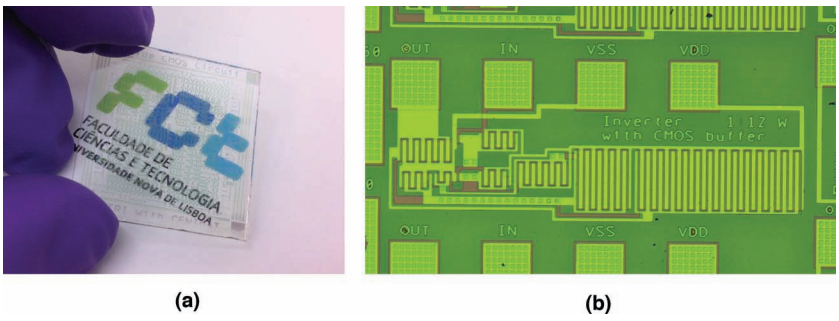
Besides TFTs, ZnO metal-semiconductor field-effect transistors (MESFETs) were used to fabricate integrated inverters, using Ag_xO Schottky diodes as level shifters, as reported by Frenzel et al.[493] in 2010. For this work, ZnO was grown by pulsed laser deposition (PLD) on sapphire substrates at 675 °C. Very low operation voltage is achieved with MESFET technology, with the inverters showing high gain values up to 197 at 3 V. The additional diode as second input allows implementing the logic NOR-function in the circuits. Oxide MESFETs seem to be quite promising for fast and low power consumption transparent integrated circuits, and GIZO was already used to fabricate MESFETs with excellent electrical properties (S = 69 mV dec^{-1} and μ_{FE} = 15 cm^2 V^{-1} s^{-1}) with a maximum temperature of 150 °C,[494] but GIZO MESFET inverters were not yet demonstrated.

Based on these initial results, a similar scenario to the one depicted for displays seems to arise regarding oxide-based circuits: transparency can be an added-value property for specific applications, but the main focus of research is on exploring the great electrical properties and low processing temperatures of oxide TFTs that allow low cost and high performance circuit fabrication, even on flexible substrates.

5.3. Oxide CMOS

All the circuit applications reported in 5.2 make use of only n-type oxide TFTs, i.e., are based on NMOS logic. However, both n- and p-type oxide TFTs are required if the fabrication of complementary metal oxide semiconductor (CMOS) circuits is envisaged. CMOS technology offers great advantages over NMOS, especially regarding power dissipation and higher density of logic functions on a chip.

Initial results on transparent CMOS inverters were already obtained at CENIMAT|I3N (this work was done in collaboration with Dr. Sang-Hee Ko Park and Dr. Chi-Sun



(a) (b)

Figure 55. a) Transparent CMOS inverters on glass; b) optical microscopy image of an oxide CMOS inverter.

Hwang from ETRI, Korea), by using the sputtered GIZO TFTs and SnO TFTs presented in section 4, with multilayer hafnium-based dielectric and IZO electrodes. At this initial stage, a passivation layer was not used. After production, the CMOS inverters were annealed at 200 °C for 30 min in air. **Figure 55** shows a 2.5 × 2.5 cm glass substrate with several transparent CMOS inverters.

The VTC for a transparent CMOS inverter is presented in **Figure 56**. The peak gain is ≈1.7, being a gain magnitude above 1 is required to sustain signal propagation in integrated circuits using inverters, such as ROs. However, even for low V_{IN} the p-type TFT has some non-negligible current flowing between source and drain, causing $V_{OUT} < V_{DD}$. The fact that the p-type TFT cannot be entirely switched off also contributes to the fact that for larger V_{IN} we have $V_{OUT} > 0$ V. A more detailed knowledge regarding how to control the subgap density of states in p-type oxide semiconductors will certainly allow to improve device and circuit performance, but even at this initial stage these results already prove that transparent CMOS circuit design is achievable using transparent oxide semiconductors with maximum (post-)processing temperatures of 200 °C.

Reports on oxide semiconductor based CMOS are fairly recent. Given that p-type oxide TFTs are still at the initial stage of research, the initial CMOS inverters were based on hybrid solutions, comprising n-type oxide TFTs and p-type organic TFTs. Dhanajay et al.[495] reported in 2008 a hybrid CMOS inverter on Si substrates based on ambipolar TFTs comprising a stack of In_2O_3 and pentacene as the channel layer. The ambipolar behaviour critically depends on the thickness and morphology of the In_2O_3 layer. Two identical ambipolar TFTs, fabricated with a maximum temperature of 750 °C, were used to build a CMOS inverter that exhibits a peak gain of 9. Still in 2008, the same authors[474] reported for the first time fully oxide based CMOS inverters, by combining p-type SnO_x and n-type In_2O_3 TFTs, being the channel layers being produced by reactive evaporation. The inverter operates at fairly high voltages and exhibits a peak gain of ≈11 (**Figure 57**).

In 2010, Yabuta et al.[477] reported the formation of both n-type SnO_2 TFTs and p-type SnO TFTs in the same substrate, by using a SiO_x capping layer on top of sputtered SnO films, which allows to fine-tune the oxygen content of the SnO film during an annealing process (300 °C), something crucial to obtain p-type behaviour in SnO. A conceptual design of a CMOS inverter based on this production method was presented (**Figure 58**a), but no actual CMOS devices were fabricated.

Following the previous paper,[477] the ambipolar effect observed in SnO films was successfully applied to a CMOS inverter by Nomura et al.[483] in 2011. But in this case, rather than using organic and oxide semiconductors,[495] only SnO was used to achieve the ambipolar behaviour, this being the first demonstration of a CMOS circuit using a single oxide semiconductor. The SnO films were deposited by PLD at room temperature on thermally oxidized Si substrates, being the final devices annealed at 250 °C. The CMOS inverter operates with a peak gain of ≈2.5 (Figure 58b). The low gain when compared with other ambipolar transistors containing channel layer of different materials such as microcrystalline silicon and organics (voltage gains 5–20) is justified by the large *off*-current and imbalance of the SnO TFTs, caused by the low μ_{FE} of the n-type SnO TFTs.

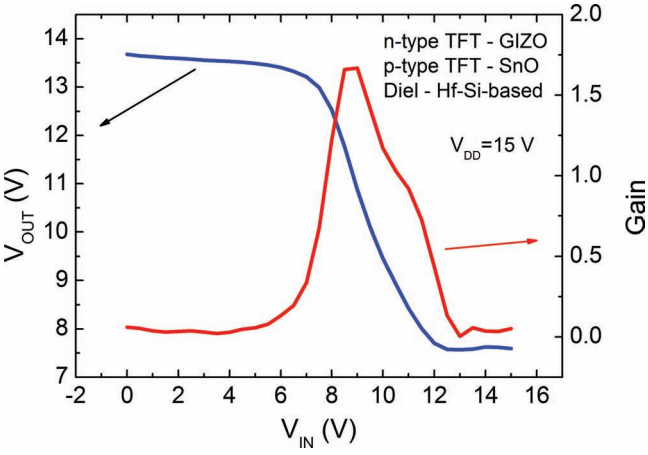


Figure 56. VTC and gain for a transparent CMOS inverter with n-type GIZO and p-type SnO TFTs fabricated at CENIMAT/I3N.

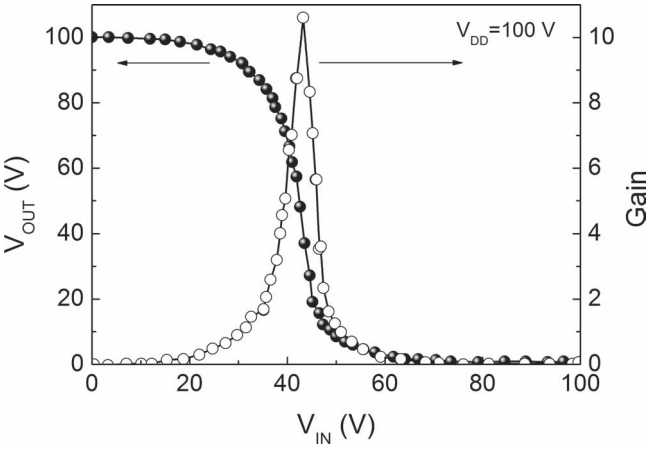


Figure 57. VTC and gain for a CMOS inverter with p-type SnO_x and n-type In_2O_3 TFTs (adapted from [474]).

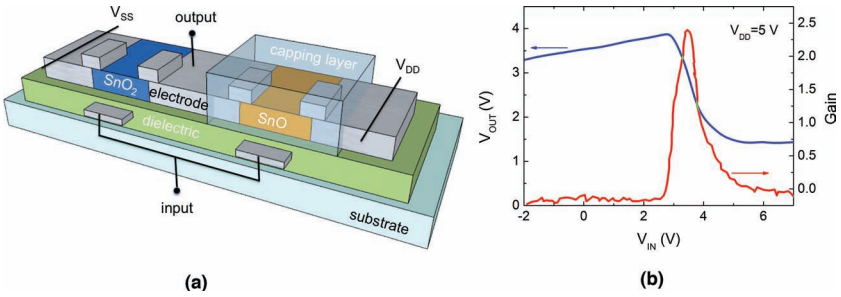


Figure 58. Schematic of a conceptual CMOS inverter using n-type SnO_2 and p-type SnO TFTs (adapted from [477]); b) VTC for an ambipolar SnO CMOS inverter (adapted from [483]).

Recently, Martins et al.[496] succeed to perform a paper-CMOS dc inverter with n- and p-type oxide TFTs using GIZO and non-stoichiometric SnO_x ($x < 2$) respectively, with an IZO gate electrode. All the layers that constitute the CMOS device were processed by reactive magnetron sputtering at room temperature. The process sequence is depicted in **Figure 59**. Both TFTs exhibit electron and hole mobilities greater than 21 $cm^2 V^{-1} s^{-1}$ and 1 $cm^2 V^{-1} s^{-1}$, respectively. As the paper itself can act as both substrate and dielectric, this means that the complexity of transferring a stand-alone electronic circuit onto a paper page is reduced. The challenge of paper electronics is to be able to produce low power consumption devices to allow densely packed integrated circuits, for a plethora of applications such as computer memory chips, digital logic circuits, microprocessors, and analogue (linear) circuits, among others, thus fueling the intended microelectronics revolution in the so-called technologies of information and communication.[497,498]

The paper-CMOS gain was 4.2 which is an encouraging value for the future prospects of paper electronics (**Figure 60**). Indeed, as illustrated by the inverter example described, CMOS on and with paper looks good; leading to the architecture of circuits naturally do not draw power and can easily be implemented as static circuits without the need for clocking circuitry, contributing today for the shaping of electronics of tomorrow.

Although in this first attempt of fabricating a CMOS device with and on paper a high leakage current is observed, it is not surprising given the advance from a rigid substrate to paper. Additionally the conventional FET gate dielectric is now replaced by paper. The use of paper dielectrics and layering of p- and n-channel FETs is highly promising. The performance of the circuit presented here does not inhibit the implementation of CMOS on paper, thus creating an opportunity for light weight, low cost and fully recyclable complementary circuits–green electronics. This is expected to create applications in disposable and recyclable electronics that range from smart labels, tags, sensors and memories to TFT driven electro-chromic paper displays, batteries[499,500] and integrated systems.

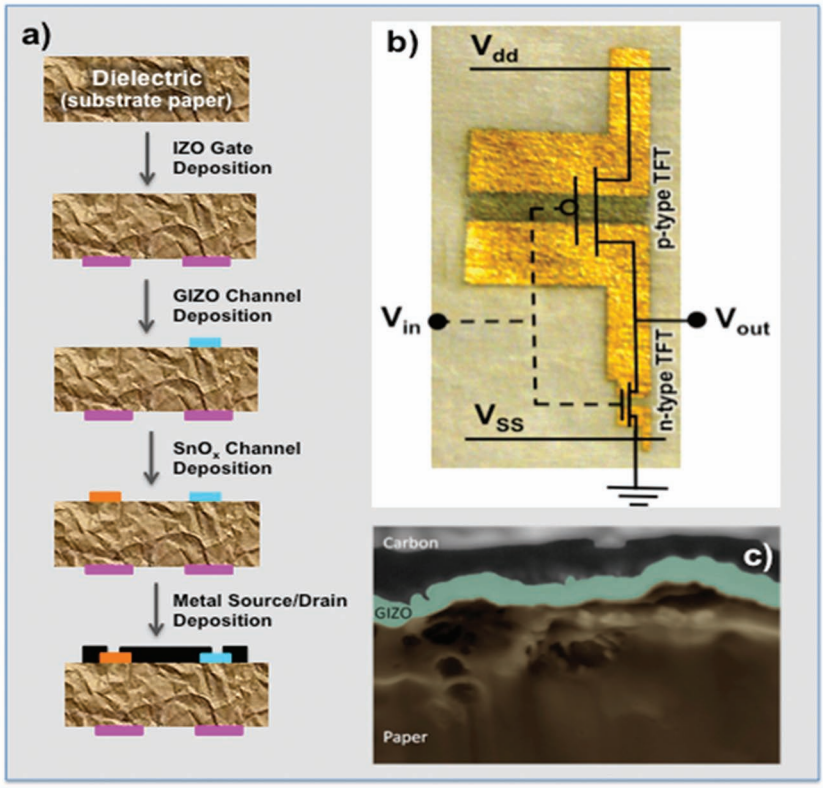


Figure 59. a) Cross sectional schematic of fabrication sequence of the paper-CMOS showing all layers that constitute the final device and how they are interconnect as well as image of the real device; b) Image of the real paper-CMOS and c) SEM cross section of the n-type paper TFT.

6. Conclusions

There has been tremendous progress in oxide based TFTs performance during the last 7 years. At present, we have reached the point where several companies such as Samsung Electronics, Samsung Mobile Display, Toppan, AU Optronics, Sharp, and LG Display have already demonstrated many prototypes of AMLCD and AMOLED panels that integrate oxide TFT backplanes and some of them have announced the mass production of flat panel displays using this new technology.

Concerning n-type oxide semiconductors, GIZO deposited by sputtering remains the best performer because of is amorphous structure and excellent electrical properties. Notwithstanding the strong advantages of oxide based TFTs, research on stability is still an open question. Besides the best dielectric material as well as dielectric/semiconductor combination, the type of TFT structure/architecture including passivation issues will play an important role in stability questions. More fundamental research includes a better understanding of the density of states and defect levels in ionic bonding

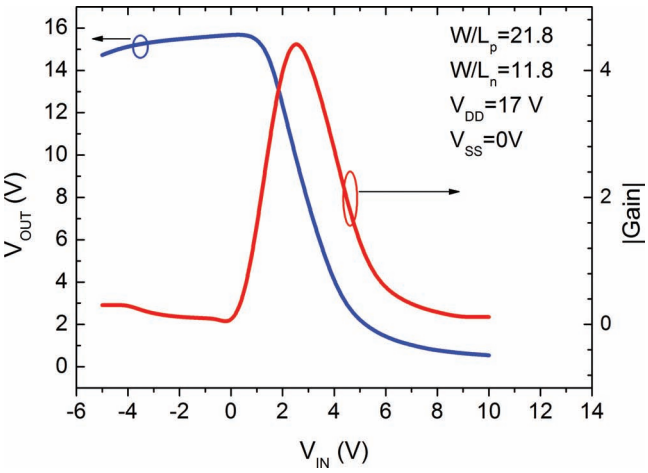


Figure 60. Voltage transfer characteristic of the paper CMOS under a V_{DD} = 17 Volts (right scale) and the CMOS gain, exceeding 4.

based semiconductors, which will lead to a more detailed understanding on the mechanisms that govern device stability.

Since 2009 substantial improvements have taken place in solution-processed oxide semiconductors, and the obtained mobilities are competing with the ones obtained trough physical techniques. The actual limitation of solution-based processes are the need to use higher temperatures, nevertheless huge achievements have been made and TFT mobilities around 10 $cm^2\ V^{-1}\ s^{-1}$ have been obtained at temperatures as low as 200 °C. Solution-based processes and novel applications will also be seriously considered in future research. This can be achieved by developing novel low-temperature chemistries and/or processes. The accomplishment of a low temperature process and reasonable device stability/reliability will be critical to the success of this new but very promising technology.

Although the performance achieved with oxide transistors processed at low temperature exceed far beyond the ones obtained with amorphous silicon and organic semiconductors, the oxides reported in the literature are mostly limited to n-type device applications, since there is a lack of p-type oxide semiconductors. Concerning the work developed so far on this topic, currently two promising candidates for p-type oxide TFTs seem to exist: copper oxide and tin oxide based semiconductors. The best results obtained are for Cu_2O and SnO with mobilities and on/off ratios of the order of 4.3 $cm^2\ V^{-1}\ s^{-1}$, 3×10^6 and 4.6 $cm^2\ V^{-1}\ s^{-1}$, 7×10^4, respectively.

Taking into account the excellent properties presented by oxide semiconductors, they are not restricted to TFTs to be used in AMLCDs or AMOLEDs display applications. Inverters, ring oscillators and CMOS inverters, either on glass, flexible and paper substrates have already been presented.

From what was already proved, oxide semiconductor based devices is today a new technology that not only may replace the conventional silicon technology in some applications but also opens new areas of applications, probably faster than you can imagine or realize!

The successful development of these new materials will require increased multidisciplinary partnerships among physicists, chemists, biochemists, and engineers.

Acknowledgements

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We would like also to thank the fruitful collaborations done directly with companies and institutes like SAIT-SAMSUNG project "STABOXI", related to the passivation of a-GIZO TFTs, Electronic and Telecommunications Research Institute of South Korea (ETRI) with the project IT R&D program of MKE - 2006-S079-03, "Smart window with transparent electronic devices" and to Saint Gobain Recherche France, for the project related to oxides for glazing.

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